

PG132-A02

370W, FH Std PCB, 384b, GDDR6x 2CH X16  
DP + DP + DP + HDMI/DP

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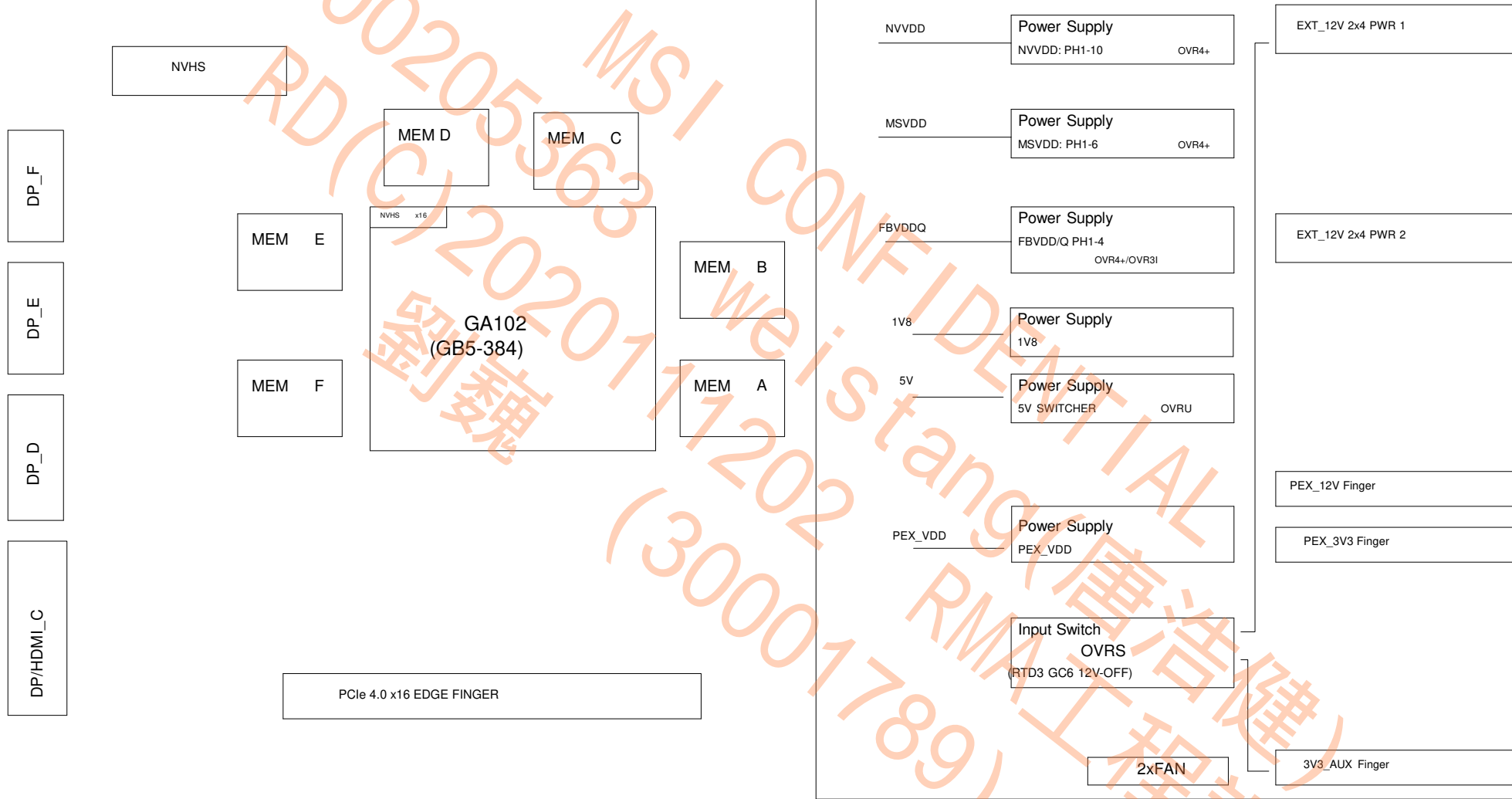
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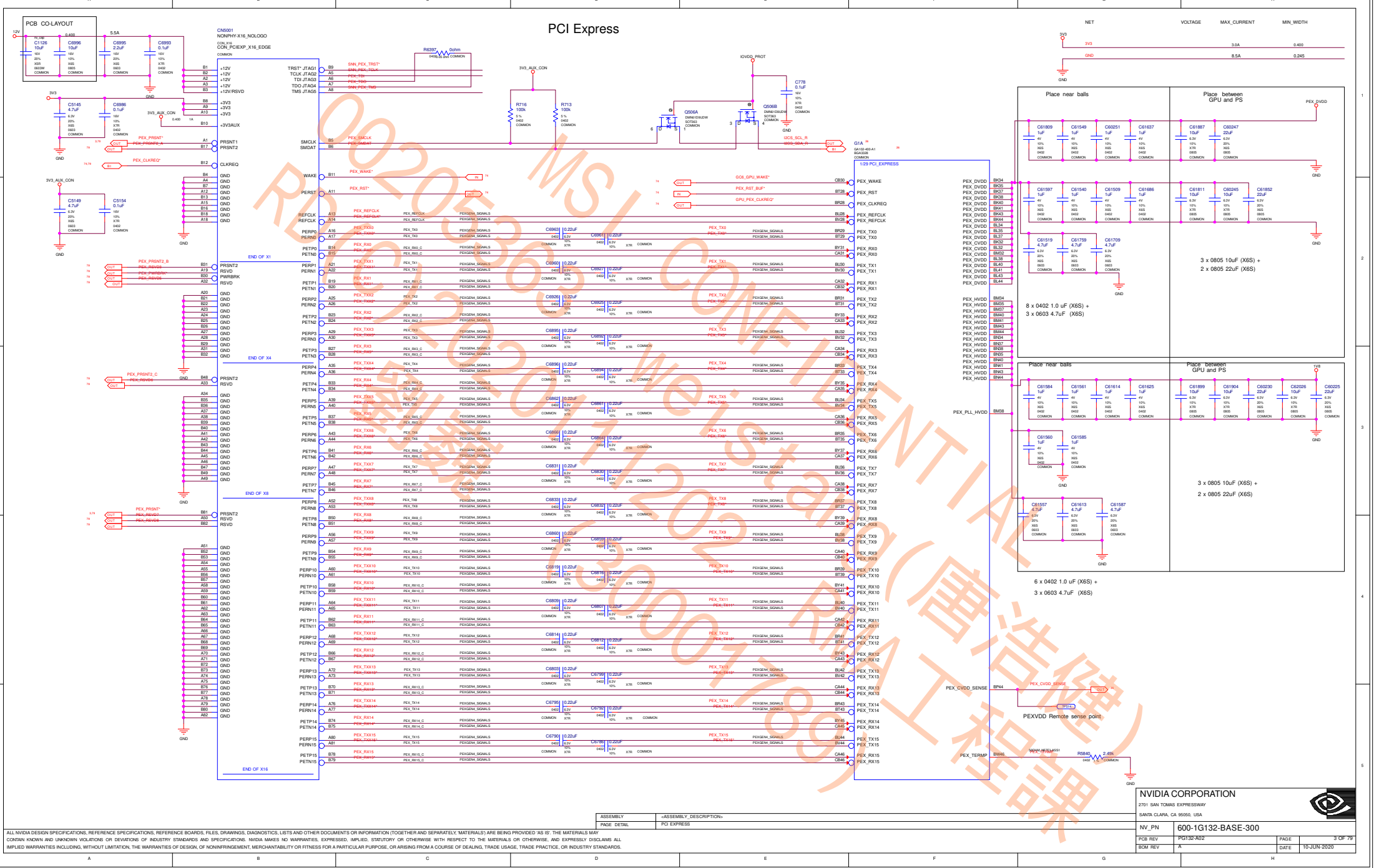
Block Diagram



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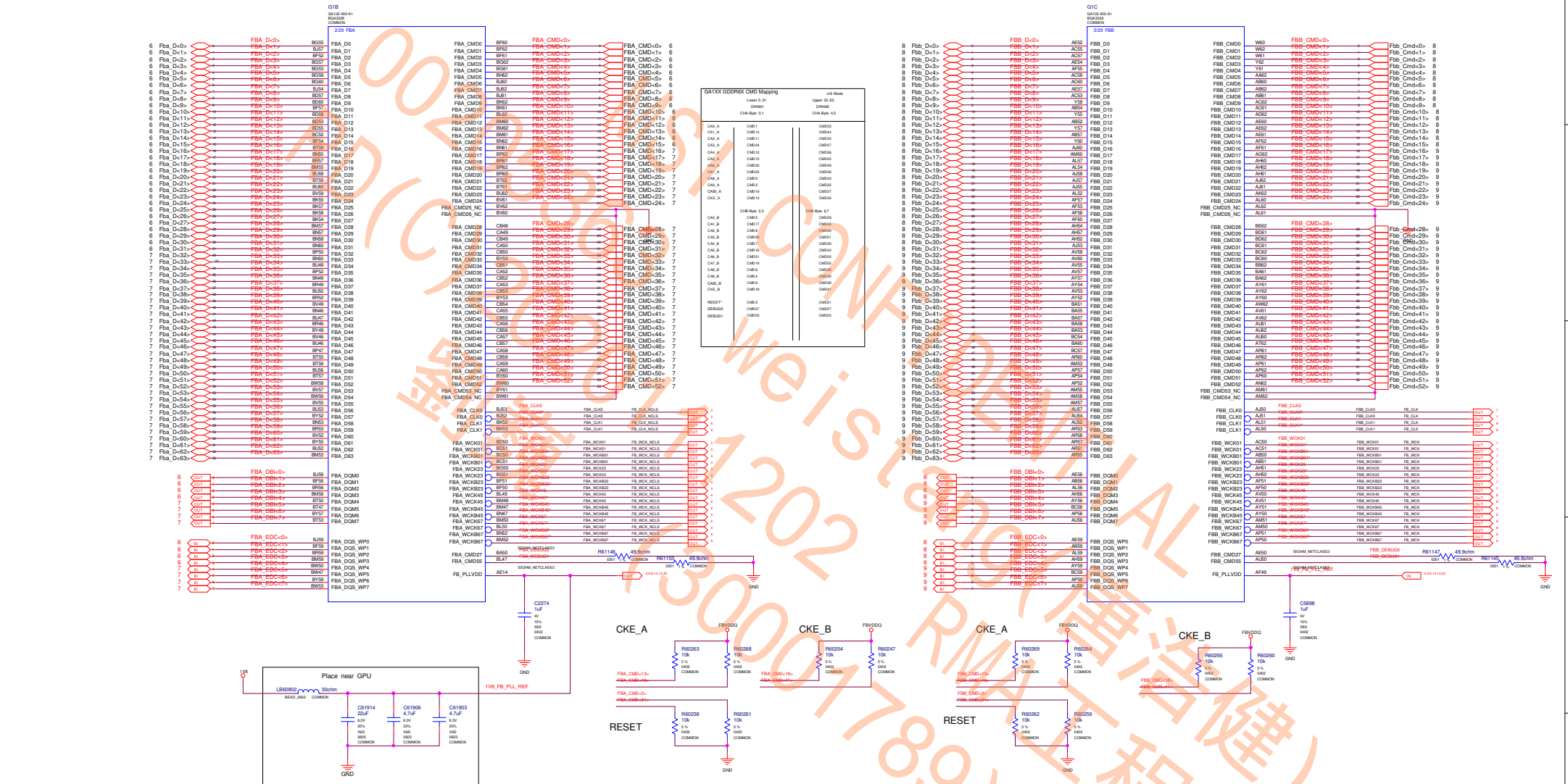
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# MEMORY: GPU Partition A/B



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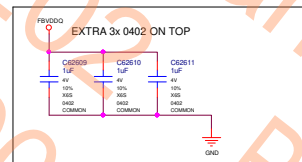
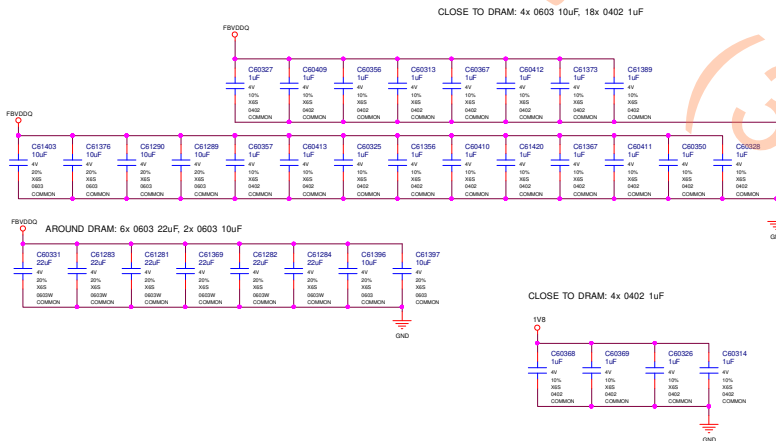
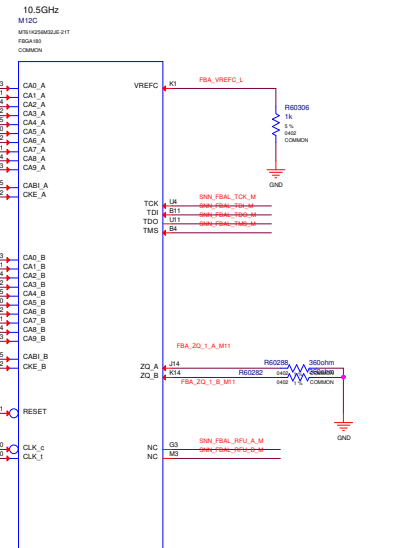
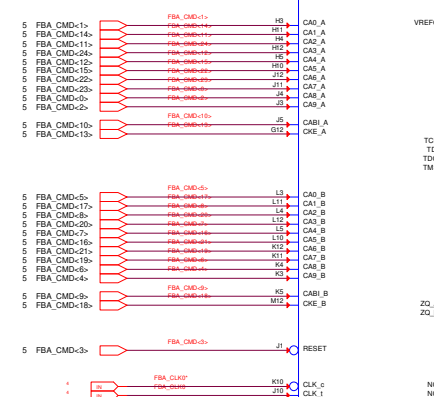
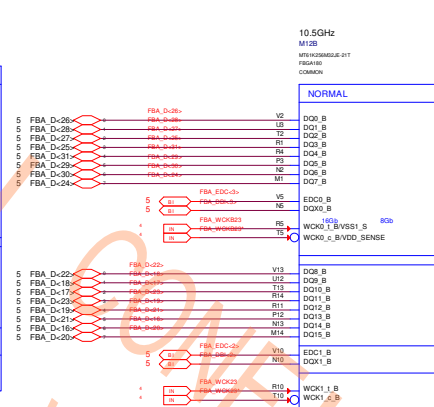
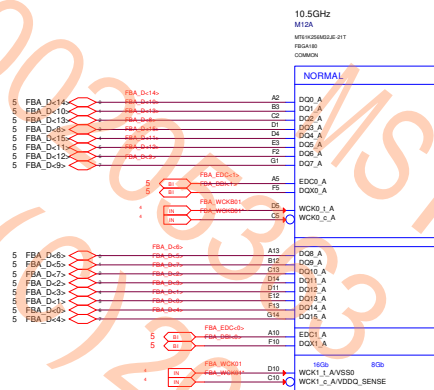
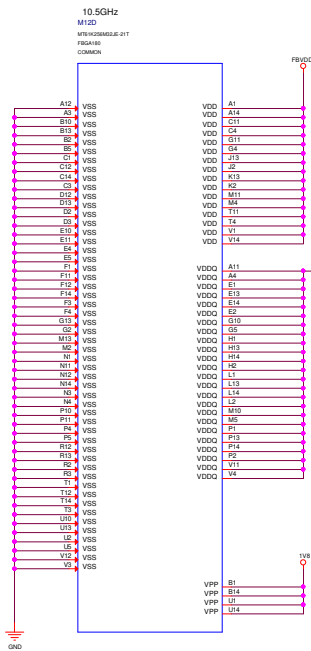
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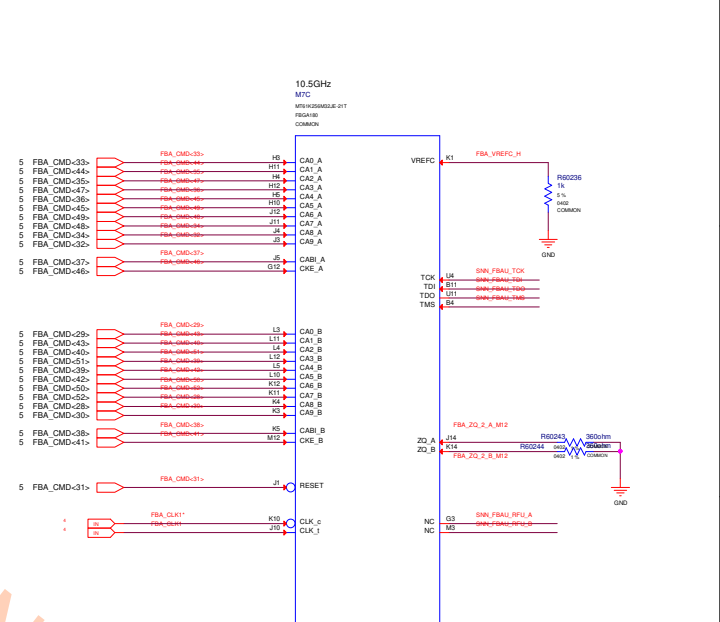
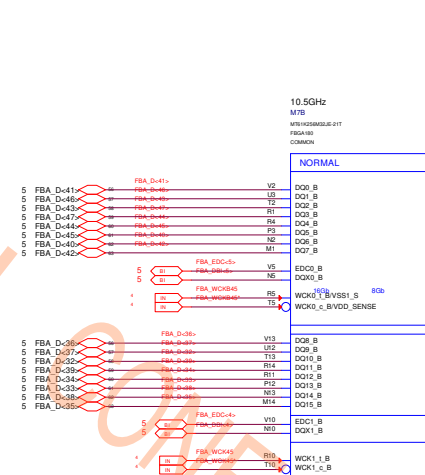
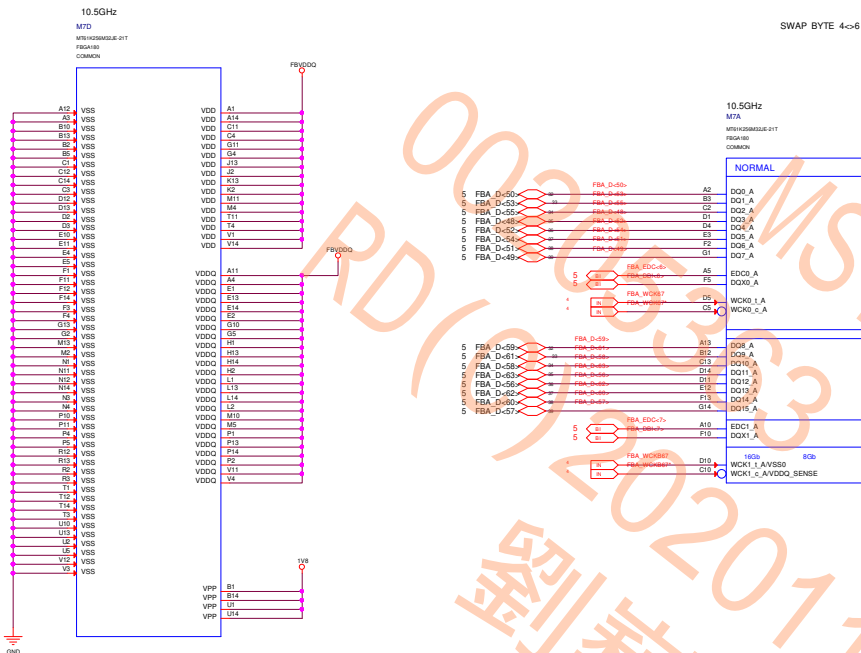
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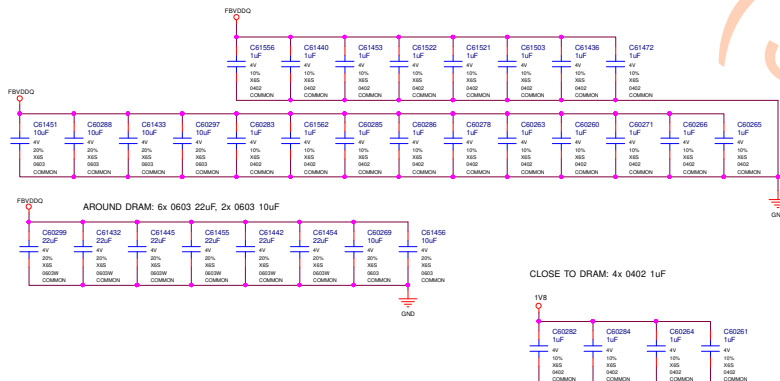
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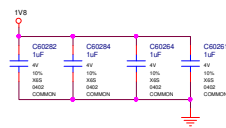
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CLOSE TO DRAM: 4x 0603 10uF, 18x 0402 1uF



CLOSE TO DRAM: 4x 0402 1uF



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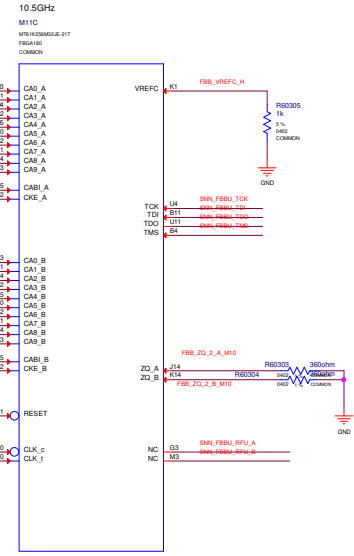
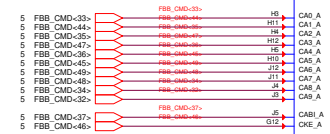
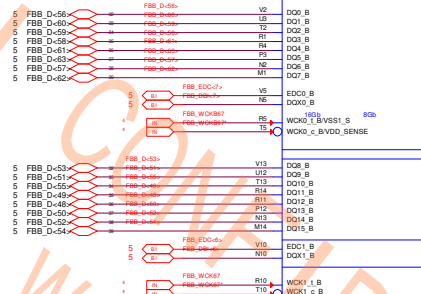
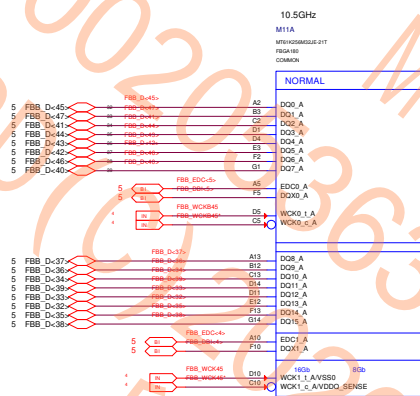
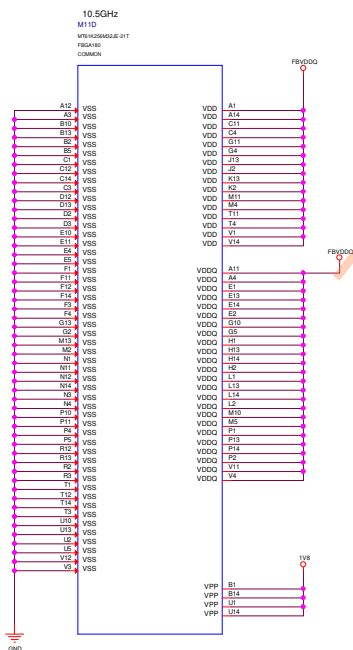
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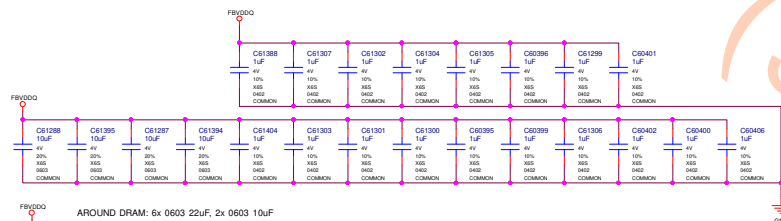




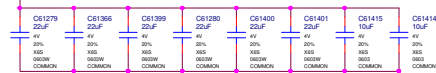
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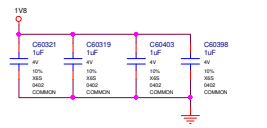
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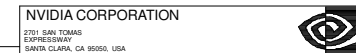
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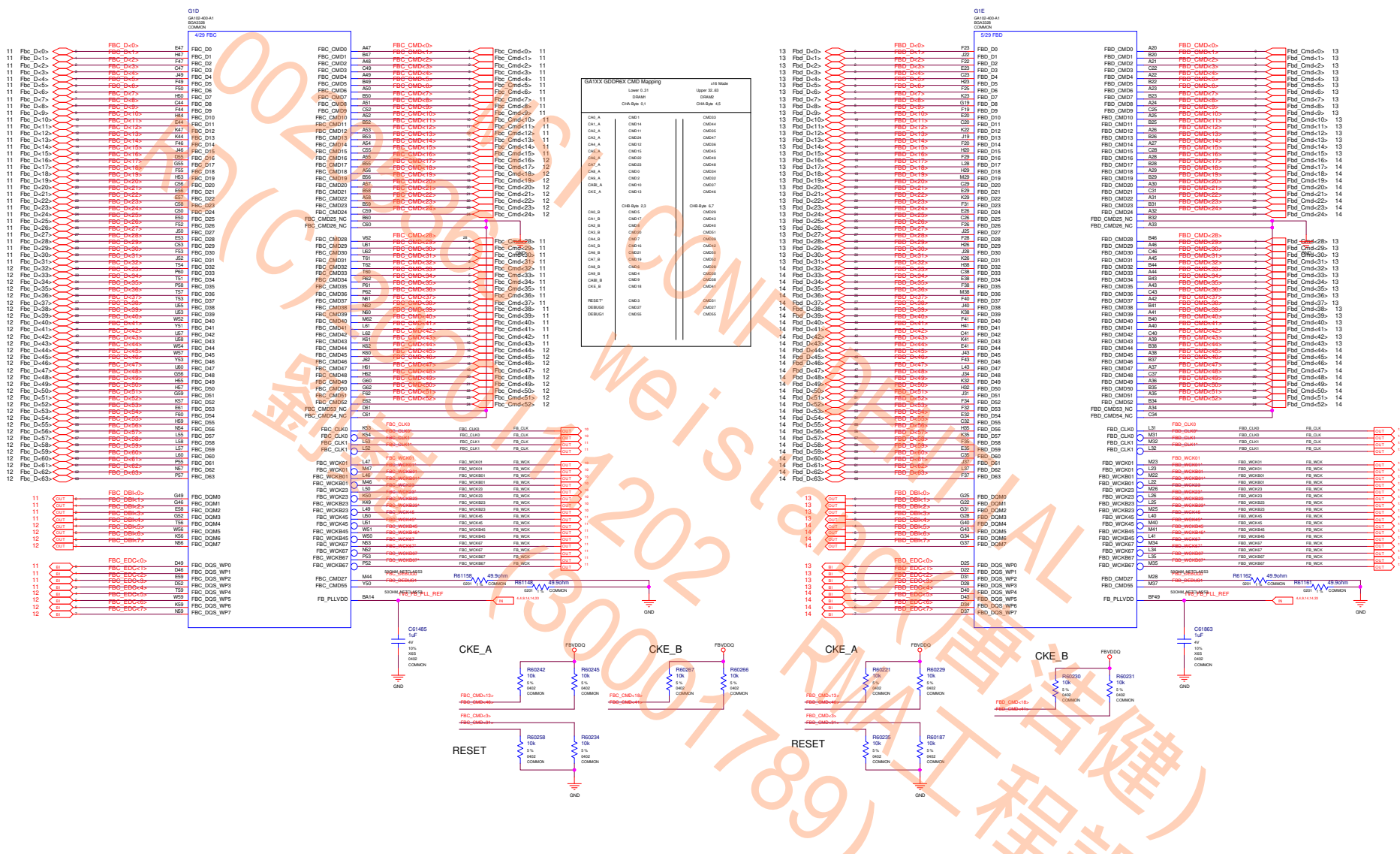
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MEMORY: GPU Partition C/D
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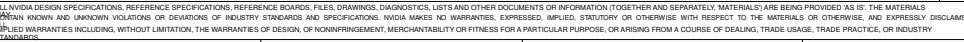
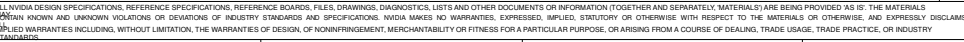
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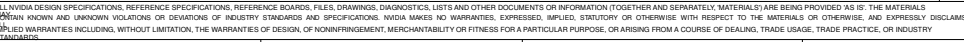
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## 10.5GHz

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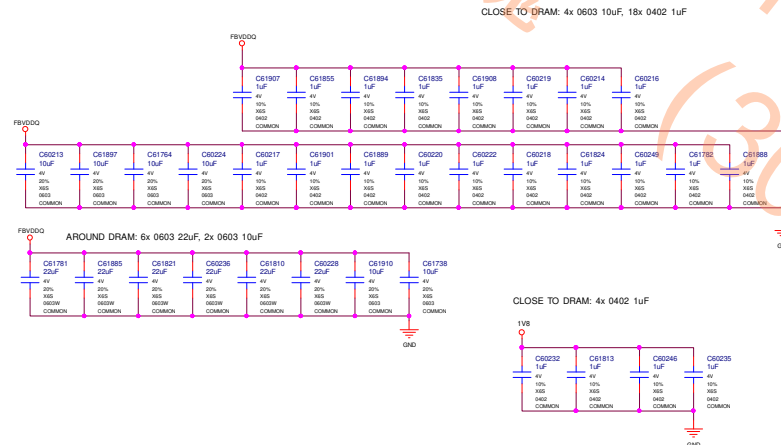
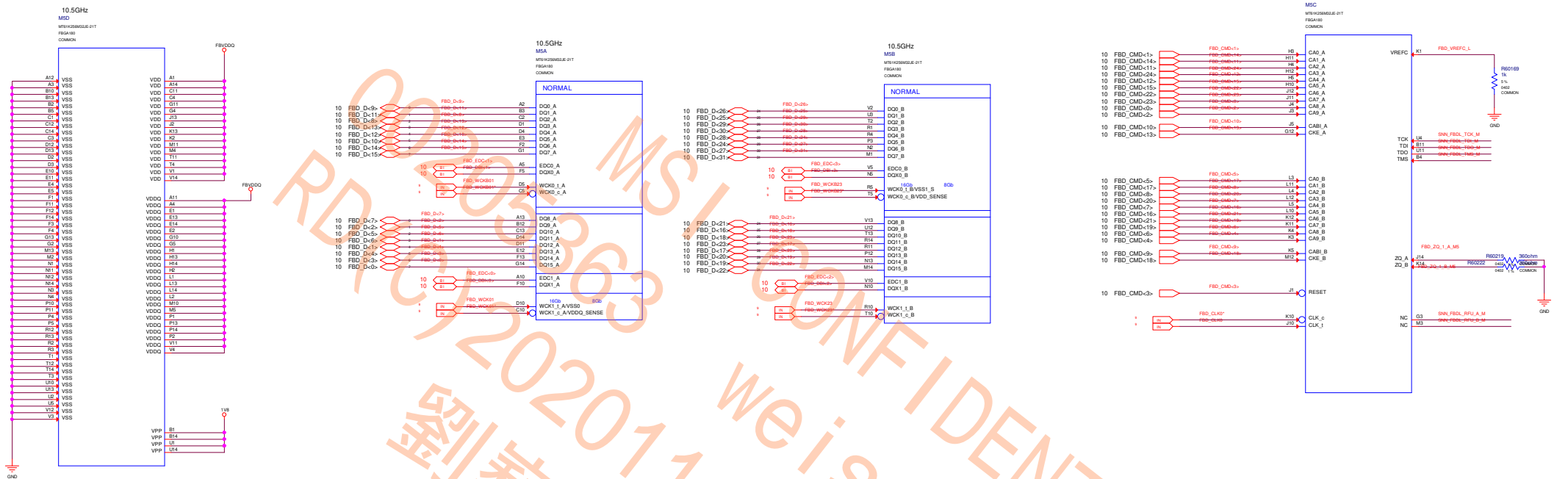
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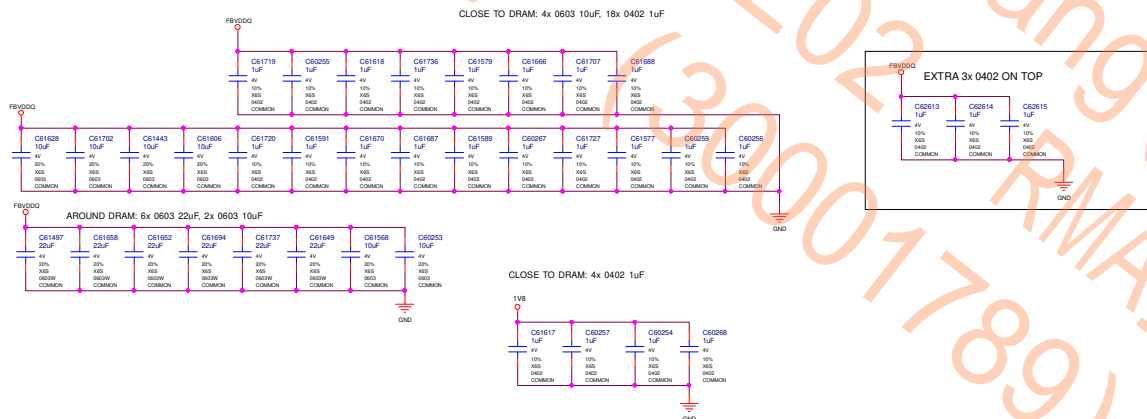
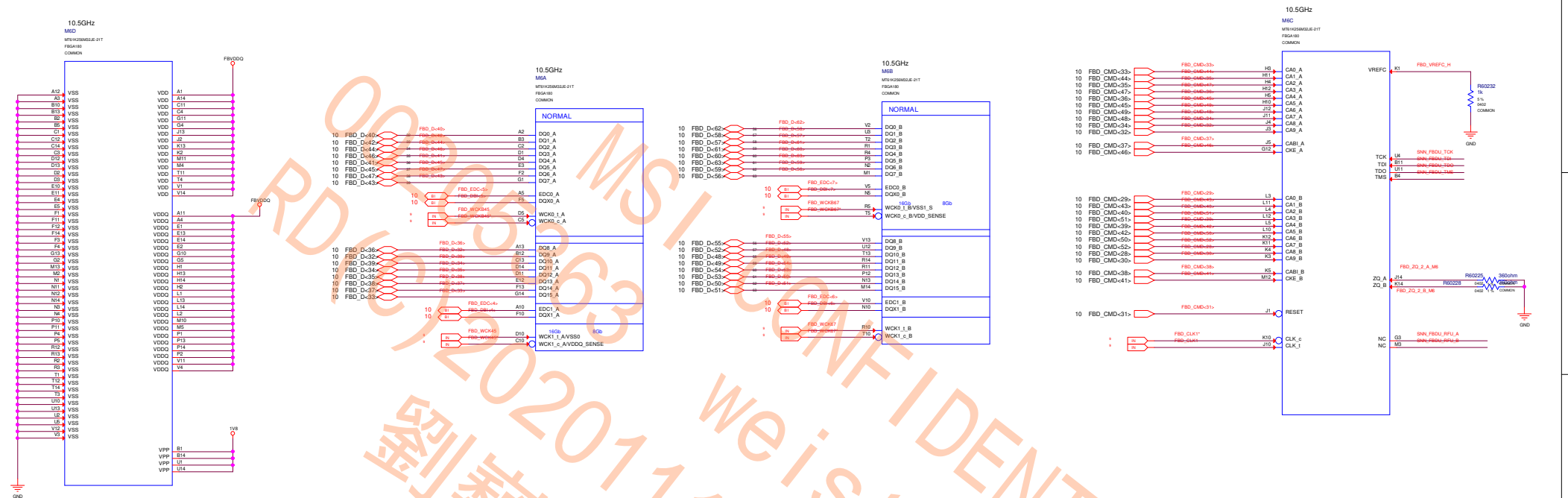
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MEMORY: FBD Partition 31..0



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## MEMORY: FBD Partition 63..32



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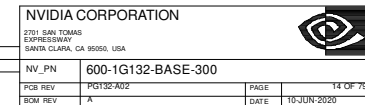
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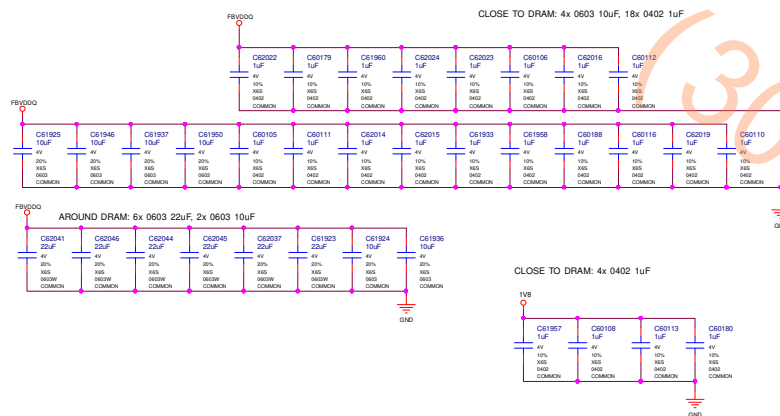
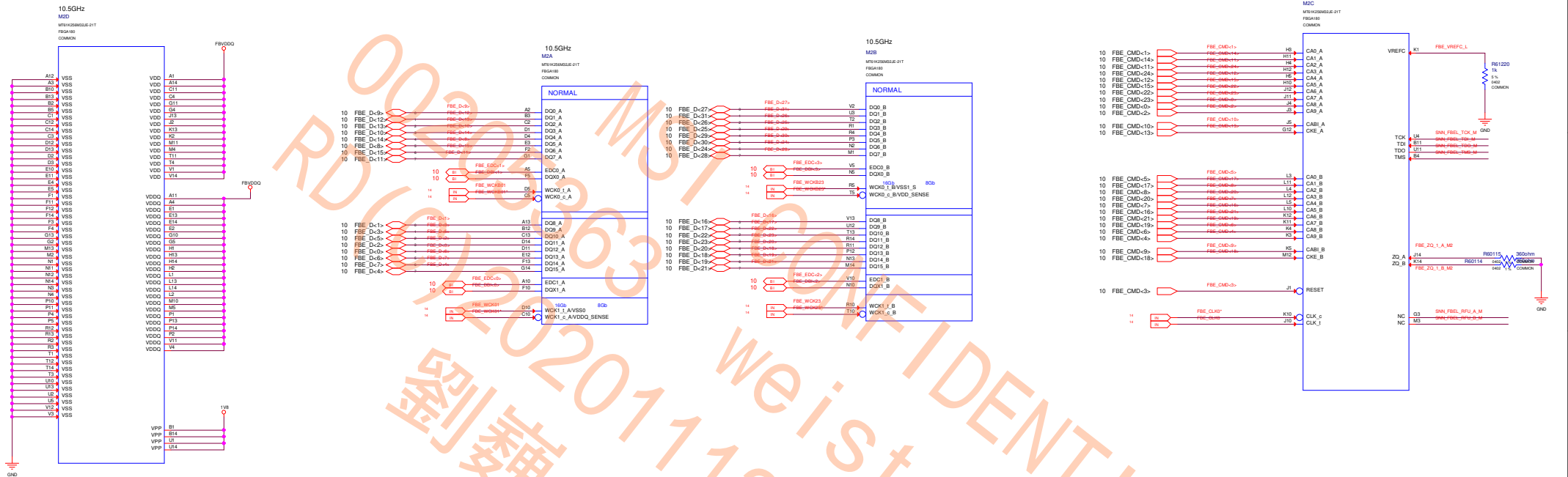
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MEMORY: FBE Partition 31..0



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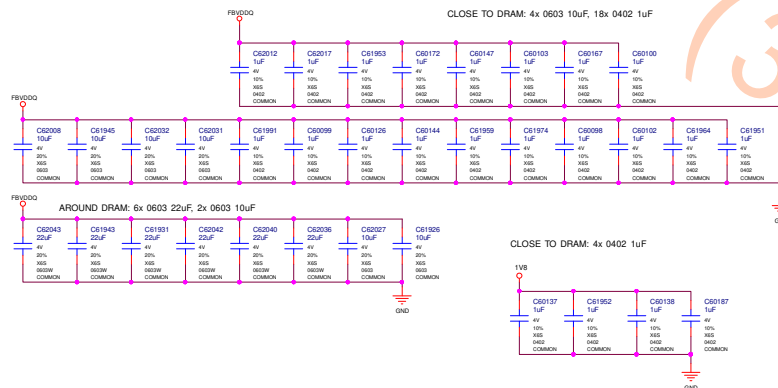
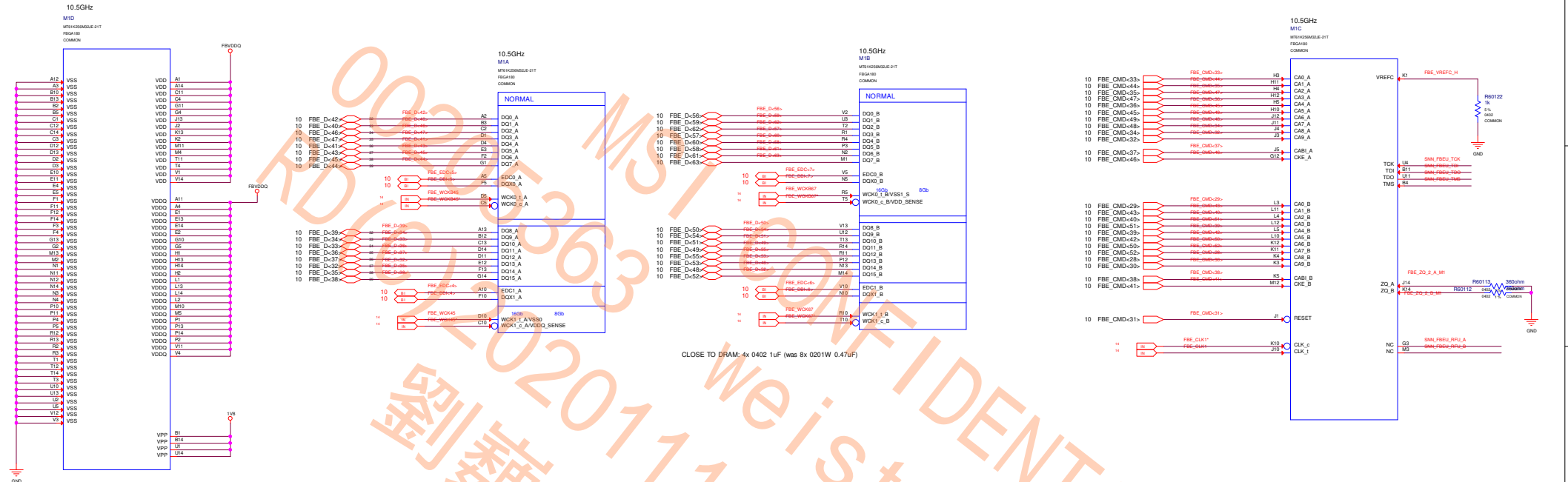


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MEMORY: FBE Partition 63..32



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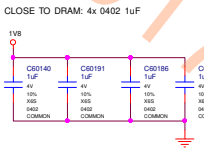
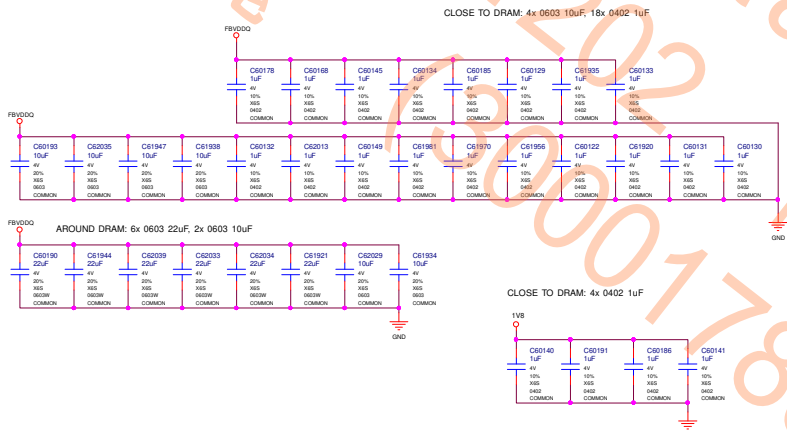
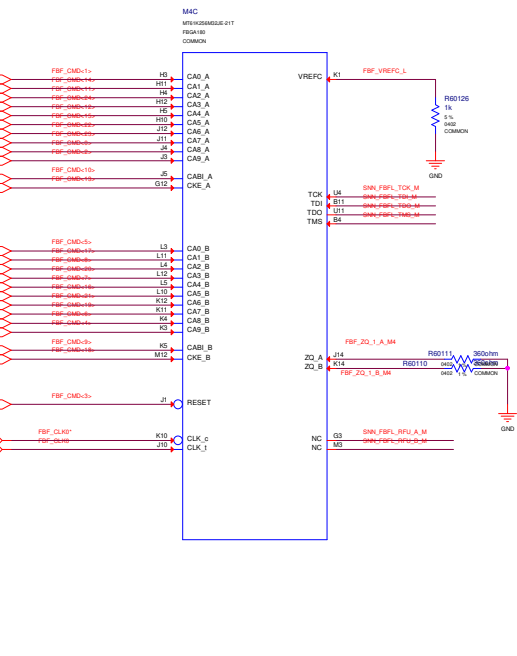
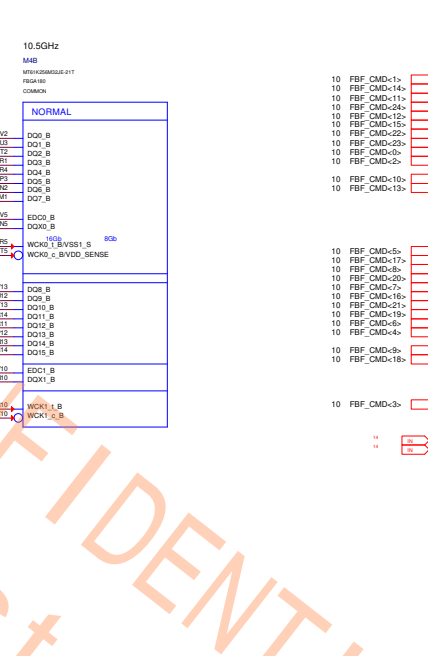
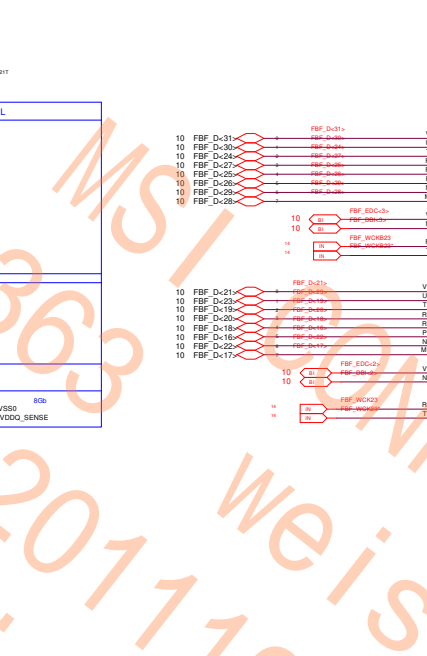
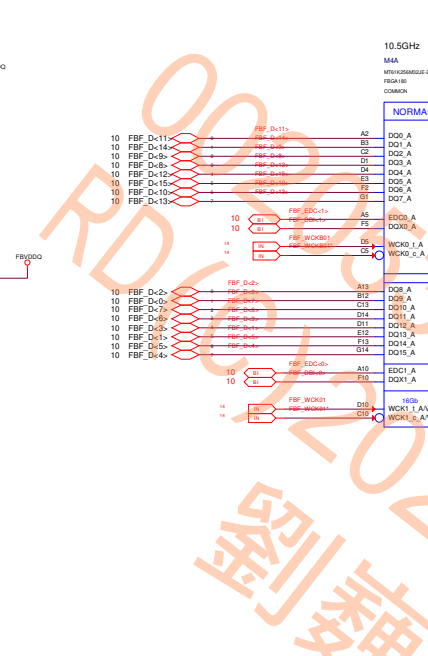
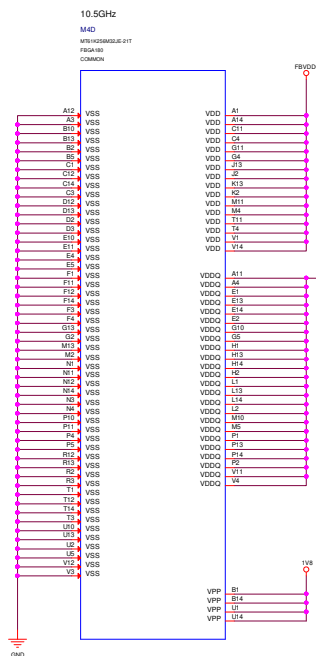
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# MEMORY: FBF Partition 31..0



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ASSEMBLY	DESCRIPTION
600-1G132-BASE-300	MEMORY: FBF PARTITION 31..0

**NVIDIA CORPORATION**

2701 SAN TOMAS EXPRESSWAY  
SANTA CLARA, CA 95050, USA

**NV\_PN** 600-1G132-BASE-300

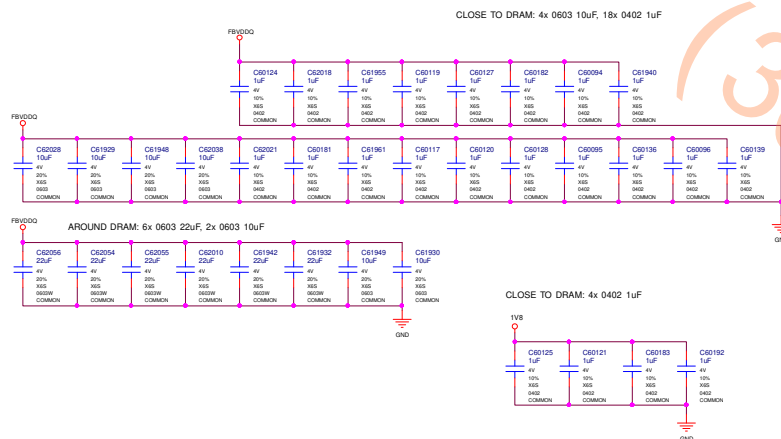
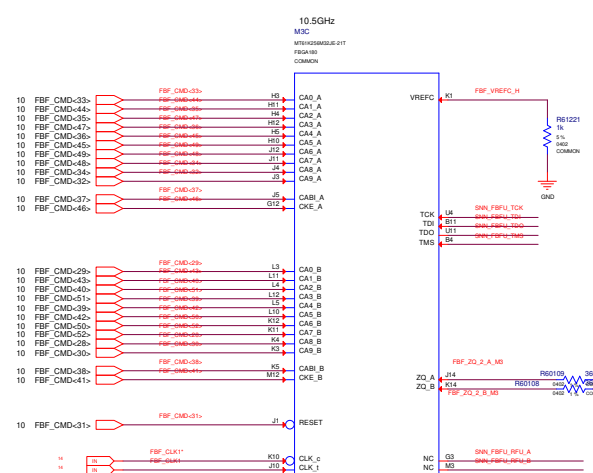
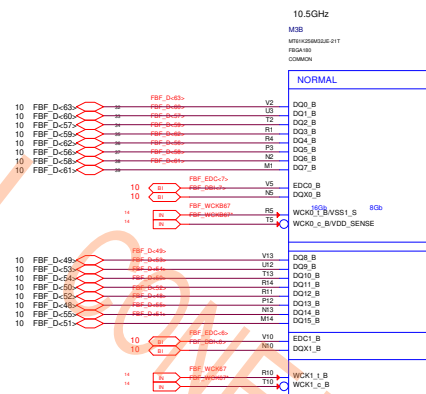
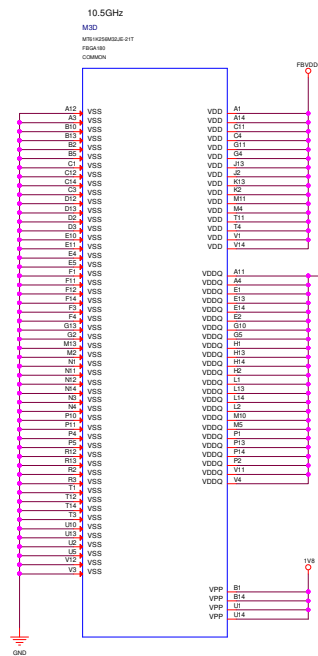
**PCB REV** PG132-A02

**BCM REV** A

**PAGE** 17 OF 79

**DATE** 10-JUN-2020

MEMORY: FBF Partition 63..32



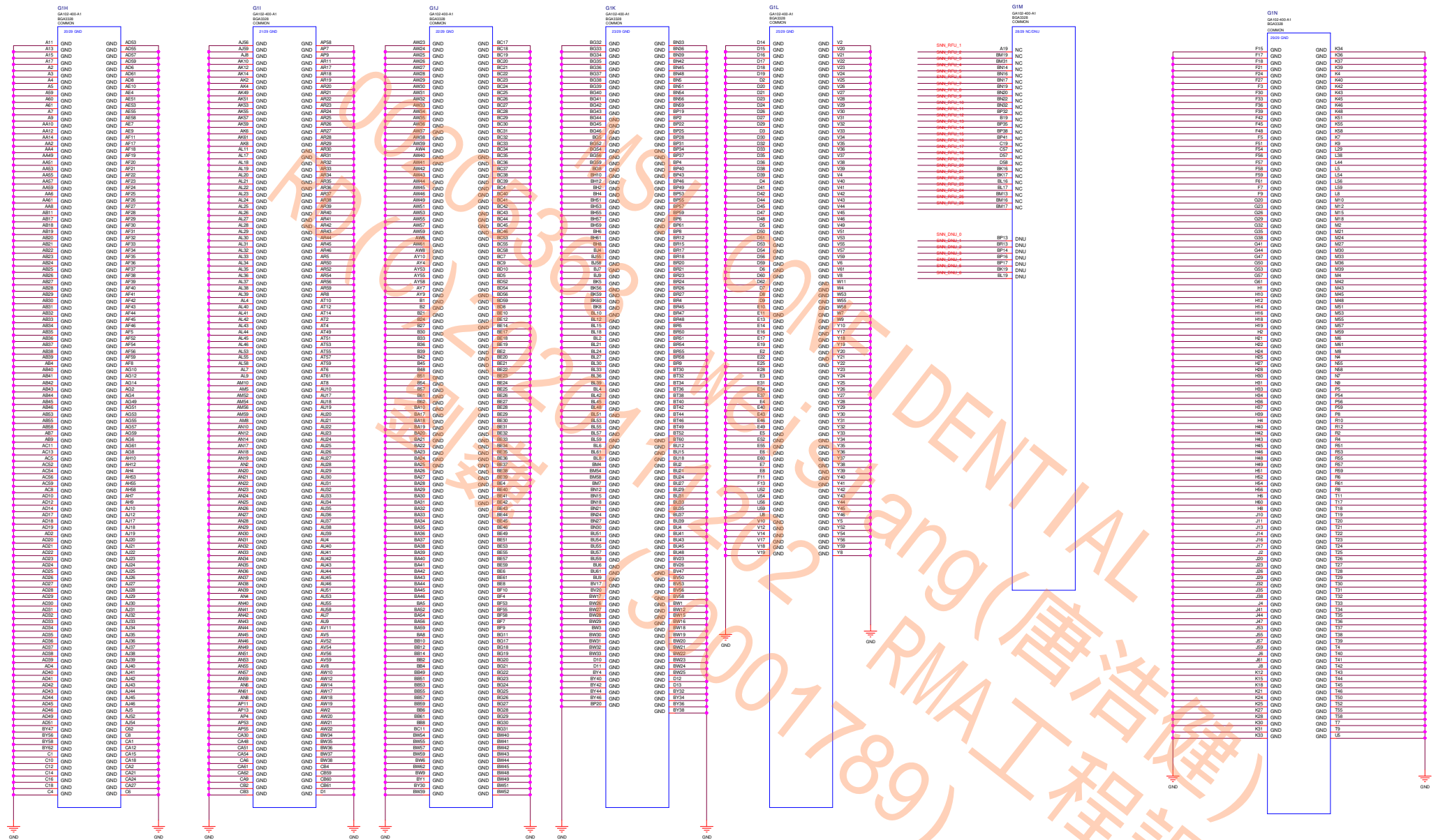
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PAGE DETAIL	MEMORY: FBF PARTITION 6332

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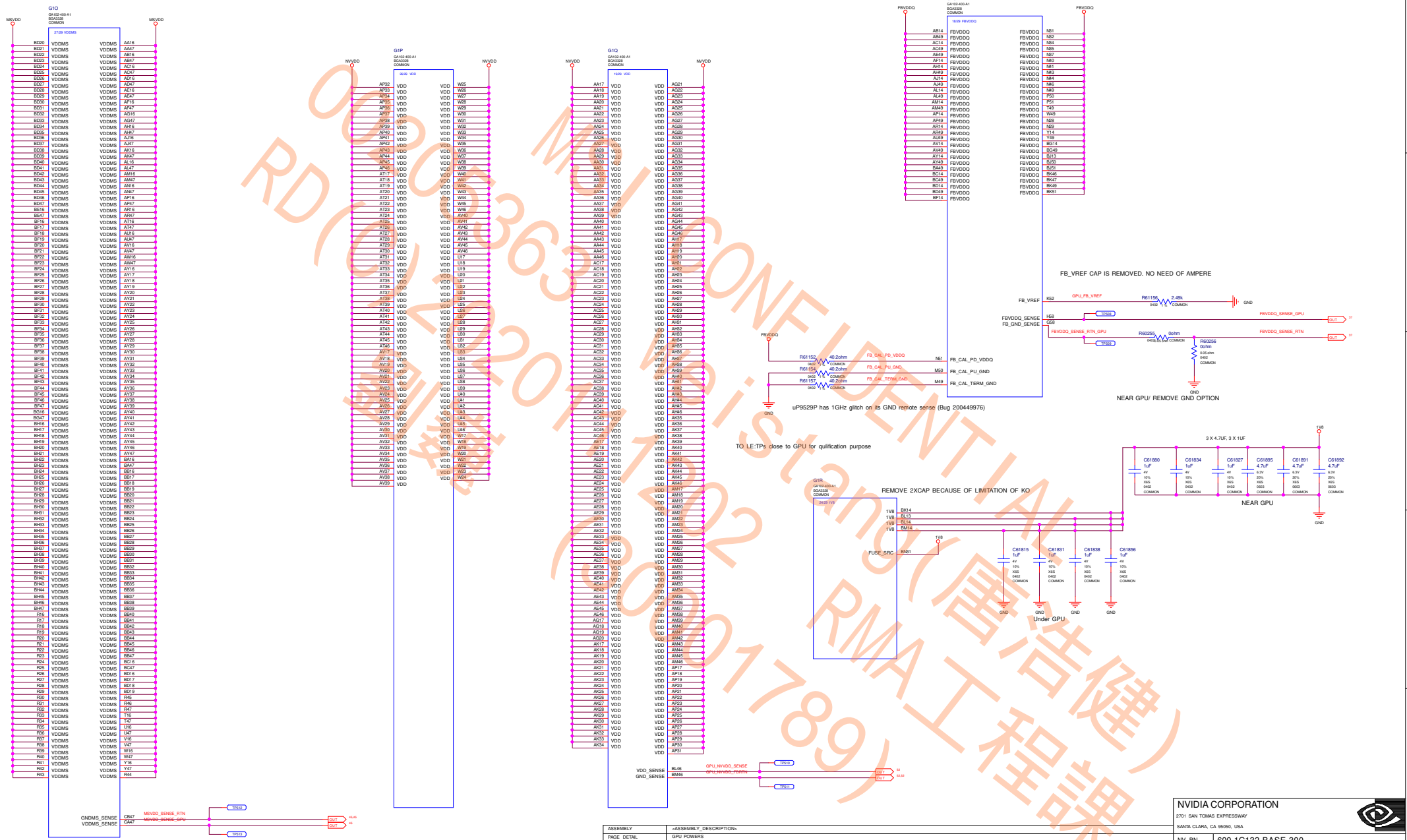


NV_PN	600-1G132-BASE-300
PCB REV	PG132-A02
BCM REV	A

## GPU GND, RFUs &amp; RSVD



GPU PWR and GND

[illegible]

ASSEMBLY	-ASSEMBLY DESCRIPTION-	SANTA CLARA, CA 95050, USA
PAGE DETAIL	GPU POWERS	600-1G132-BASE-300
IT		
CLAIMS ALL STANDARDS.		
	REV PN	PG132-A02
	DATE	18-JUN-2020

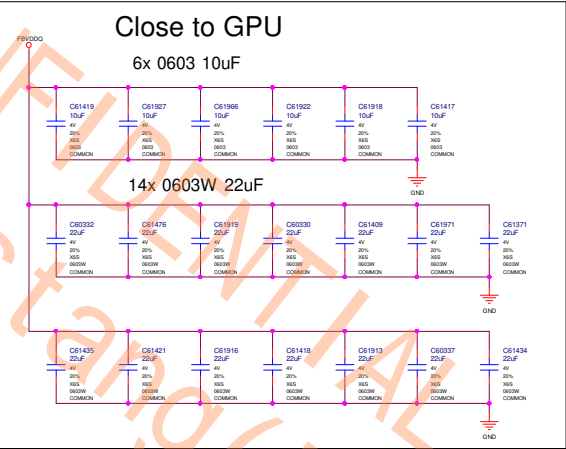
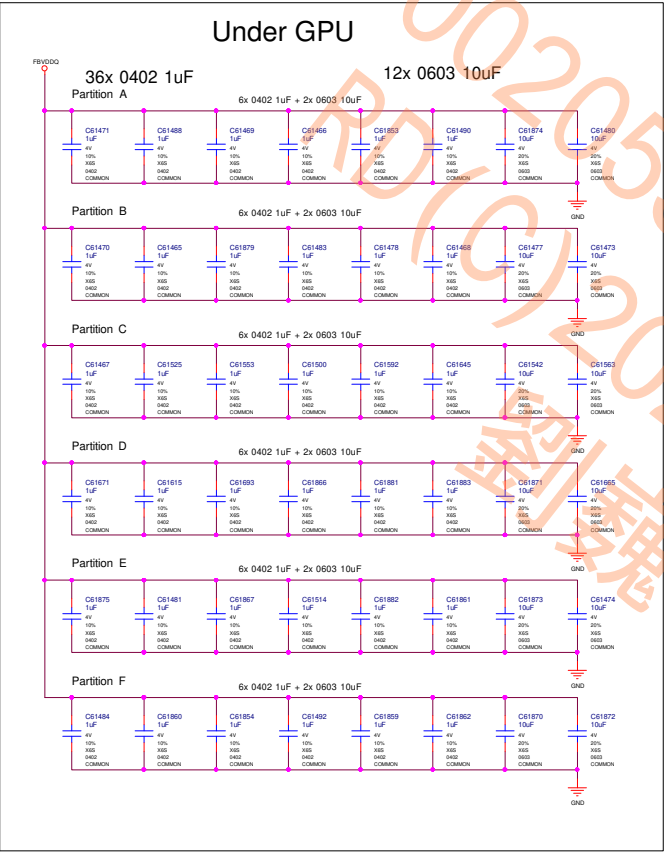


NVVDD UNDER GPU



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FBVDDQ



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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE: DETAIL	GPU DECOUPLING FBVDDQ

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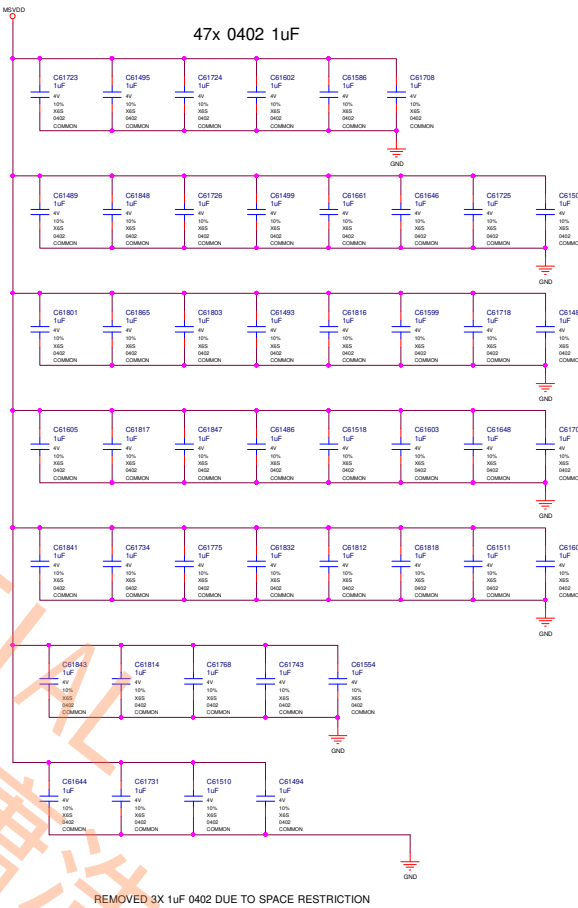
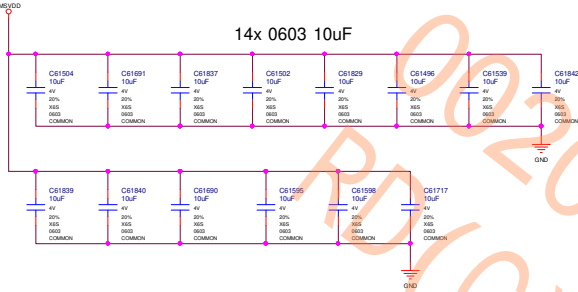


NV_PN	600-1G132-BASE-300
PCB REV	PG132-A02
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DATE	10 JUN 2020

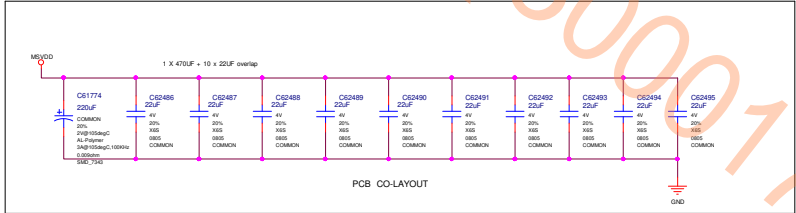
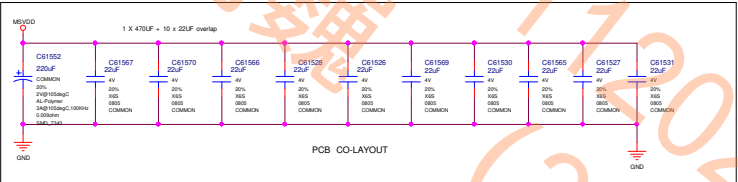
A B C D E F G H

MSVDD

UNDER GPU



2x SMD7343 220uF (EACH CO-LAYOUT WITH 10x 22uF 0805)



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ASSEMBLY	ASSEMBLY DESCRIPTION
PCB DETAIL	GPU DECOUPLING MSVDD

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600-1G132-BASE-300

PCB REV

PG132-A02

BCM REV

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DATE


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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE: DETAIL	BLANK

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NV_PN	600-1G132-BASE-300		
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# NVHS Interface and FRAME LOCK



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ASSEMBLY	ASSEMBLY DESCRIPTION
PG132-002	NVHS X16

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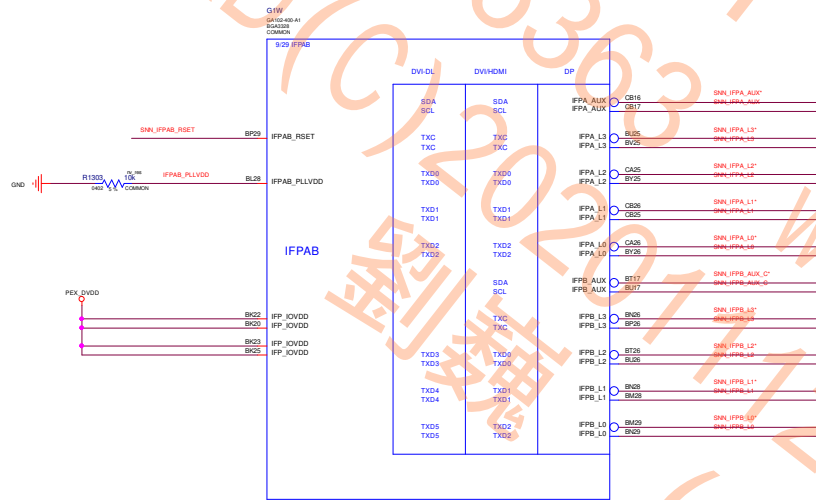


NV_PN	600-1G132-BASE-300
PCB REV	PG132-002
BCM REV	A
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IFPA UNUSED, IFPB UNUSED

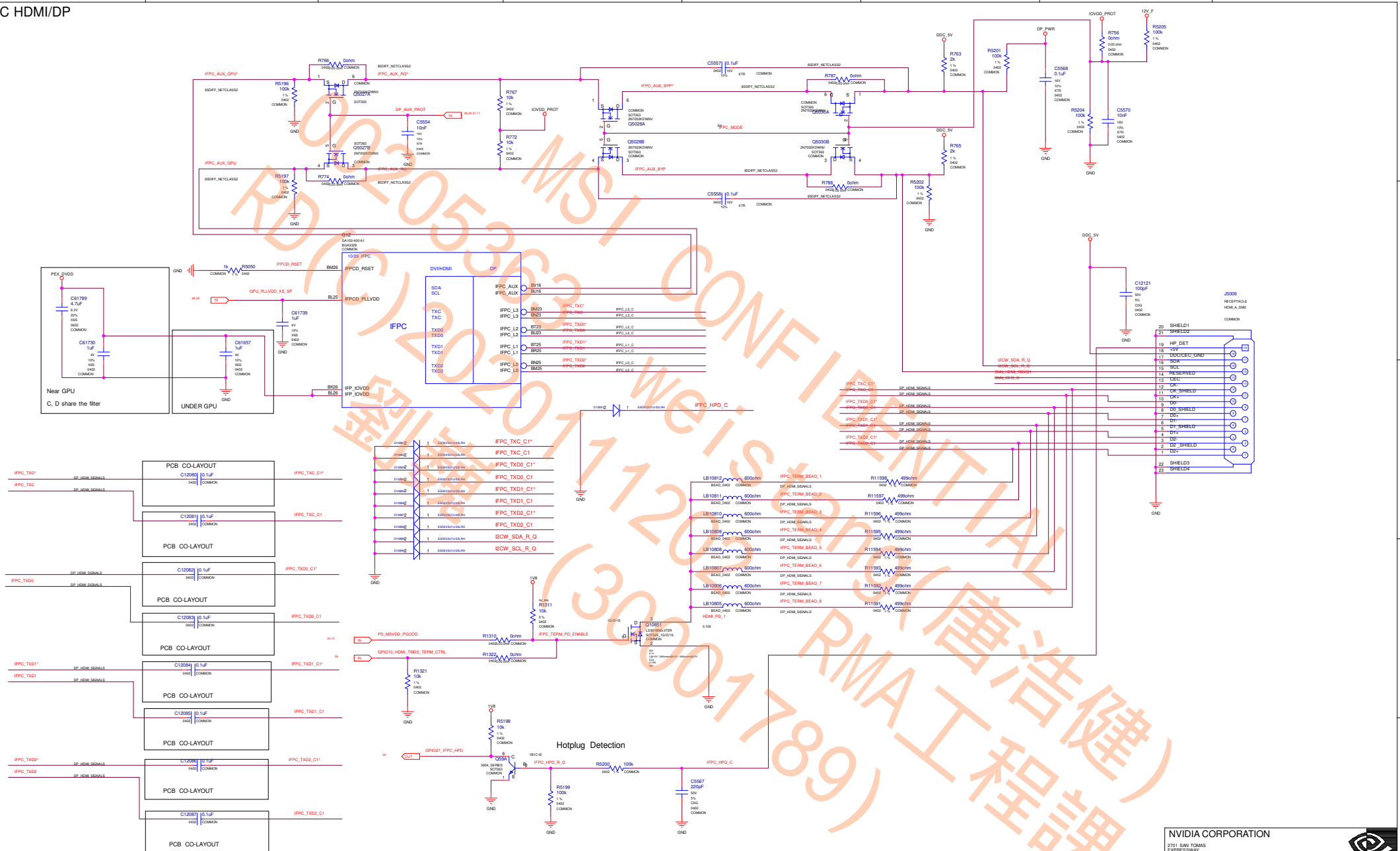


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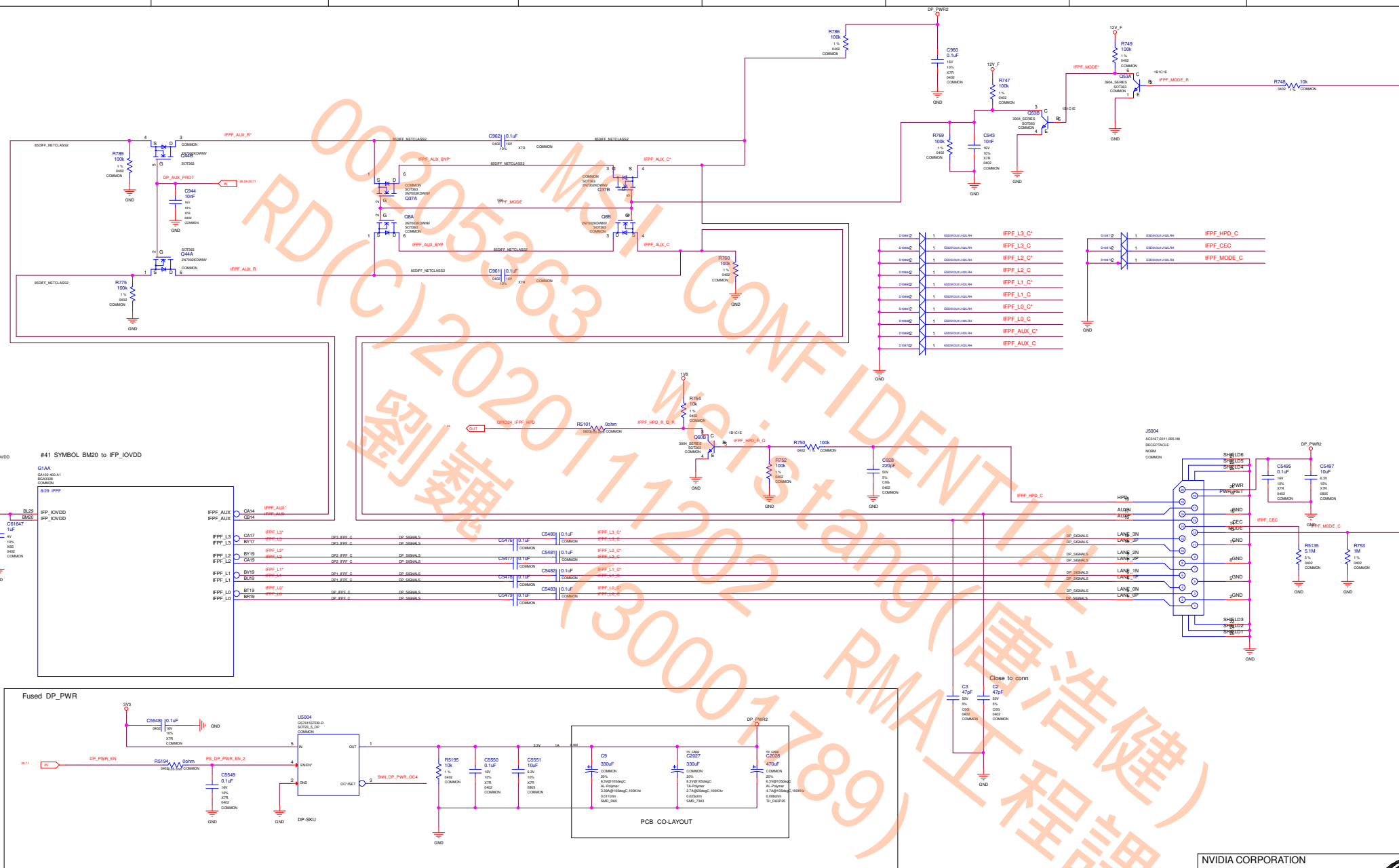


## IFPC HDMI/DP



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ASSEMBLY		ASSEMBLY DESCRIPTION:		SANTA CLARA, CA 95050, USA	
PAGE DETAIL		WPC MEMOIF		NV_PN 600-1G132-BASE-300	
DISCLAIMS				PCB REV PG132-A02 PAGE 30 OF 79	
				BOM REV A DATE 10-JUN-2020	



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MISC: ROM, Straps

GROUP0	STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
	L	L	L	00000	RAMCFG MICRON 8Gb G6X 19Gbps x16 (161-0430-900)
	H	L	L	00100	RAMCFG MICRON 8Gb G6X 19Gbps x8 (161-0430-900)
	H	L	H	00101	RAMCFG MICRON 8Gb G6X 21Gbps x8 (161-0431-900)
	L	L	M	01000	RAMCFG MICRON 8Gb G6X 20Gbps x16 (161-0424-900)
	L	L	H	00001	RAMCFG MICRON 8Gb G6X 21Gbps x16 (161-0431-900)
	L	M	H	01010	RAMCFG MICRON 8Gb G6X 19Gbps x16 (161-0430-900)

ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0]/FS_OVERT	1:ENABLE 0:DISABLE
H	H	H	0111	FS_OVERT ENABLE
L	L	L	0000	FS_OVERT DISABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
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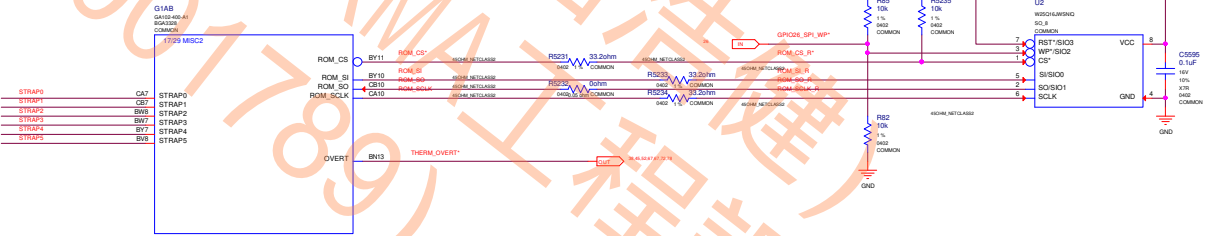
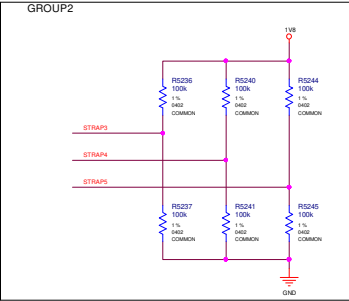
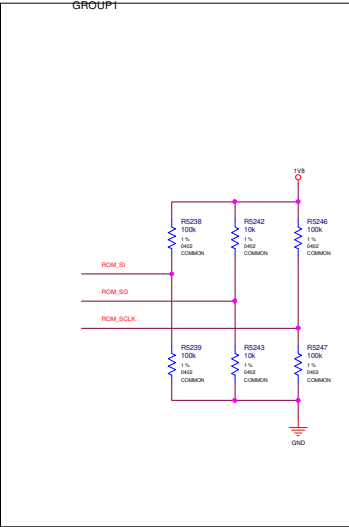
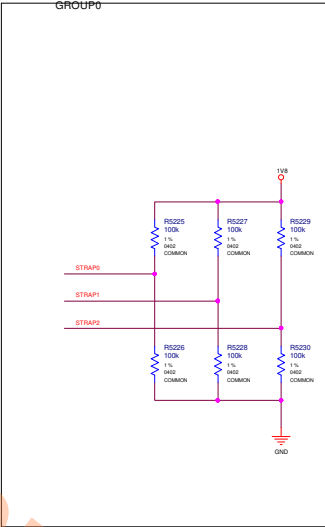
Default

H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

<-A01 PCB

<-OLD

<-LATEST A02 PCB



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PCB REV

PG132-A02

PCB REV

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PAGE

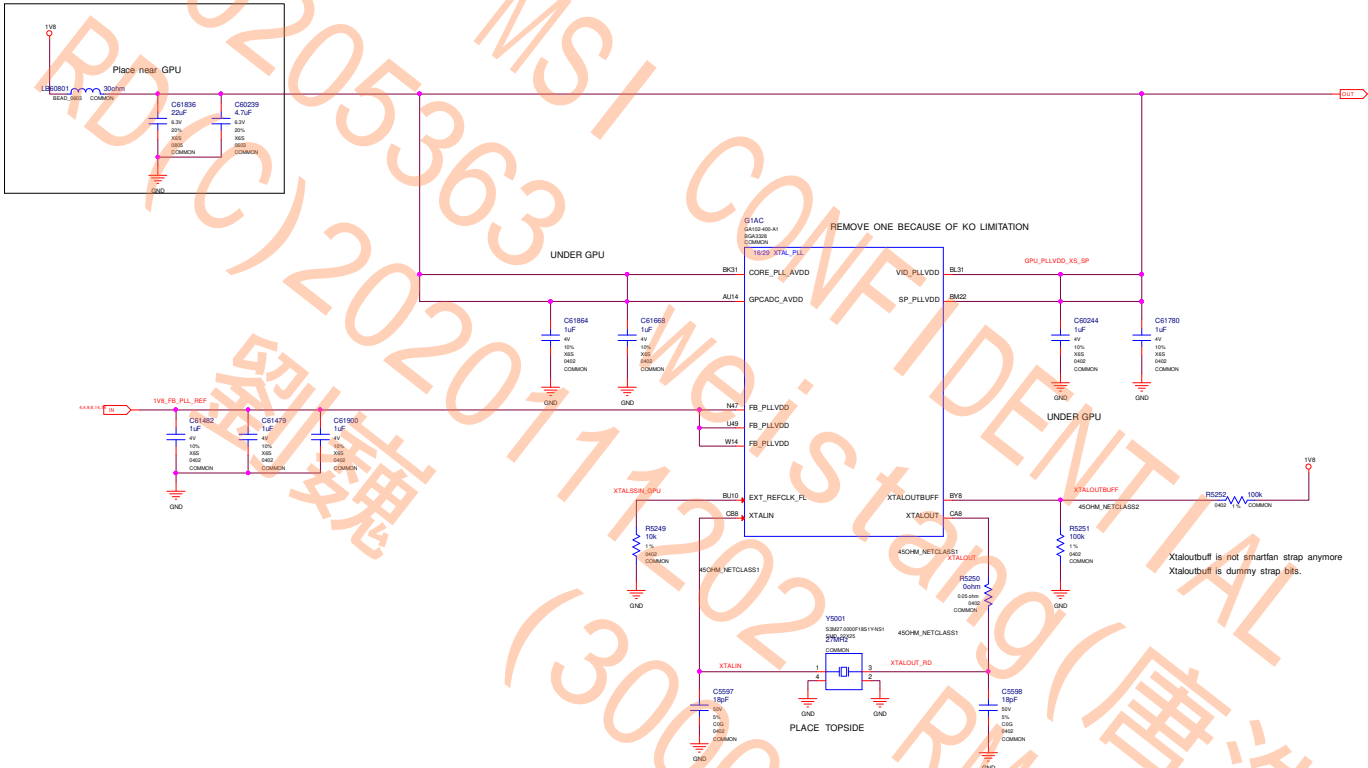
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DATE

10-JUN-2020

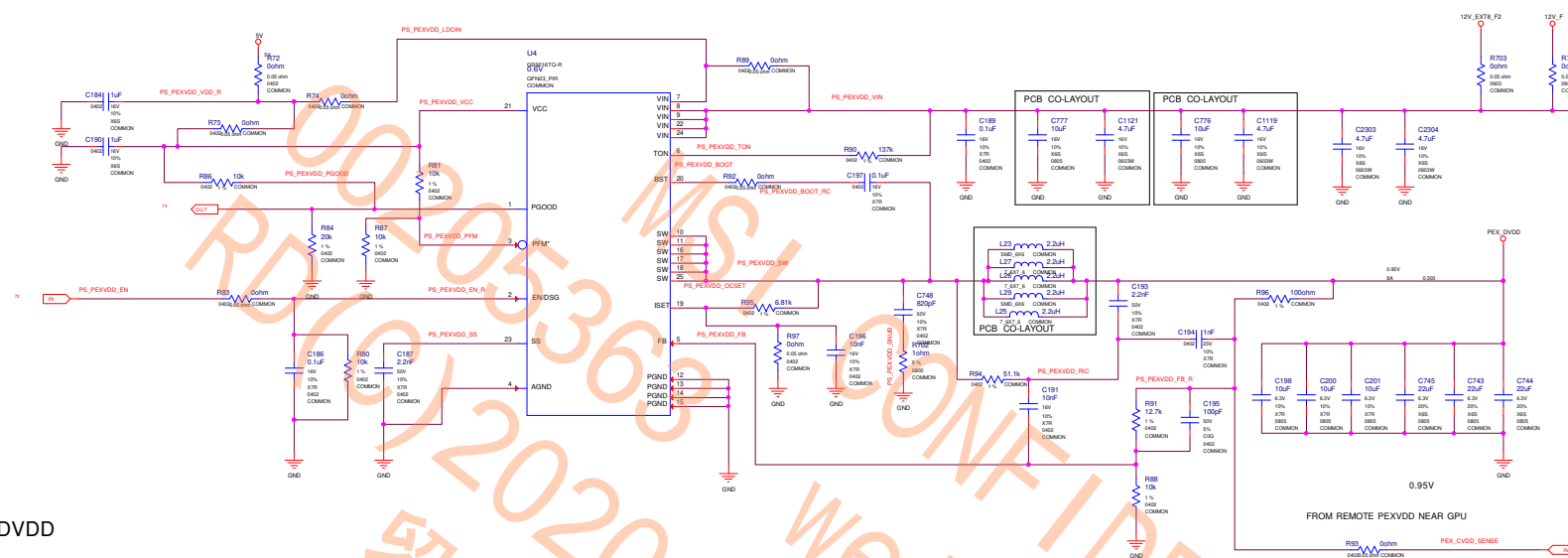
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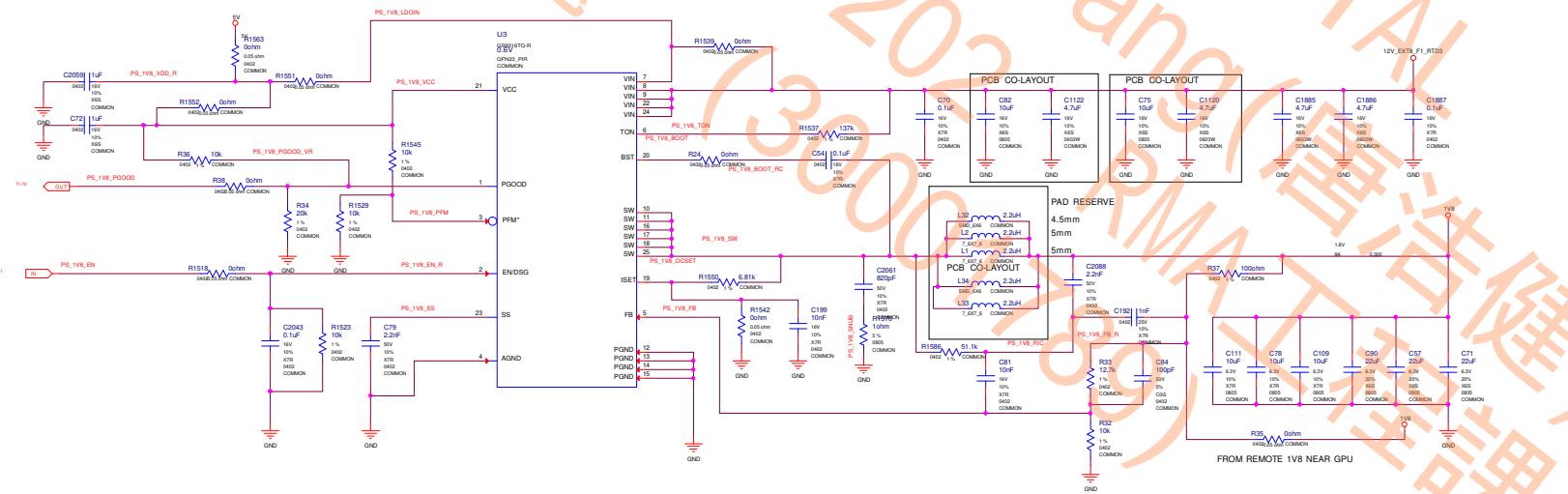


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PEX\_DVDD



1V8

ASSEMBLY	«ASSEMBLY» DESCRIPTION
PAGE DETAIL	PS: PEX_DVDD and 1V8

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NV PN	600-1G132-BASE-300
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PCB REV	PG132-A02	PAGE	35 OF 79
BCM REV	A	DATE	10-JUN-2020

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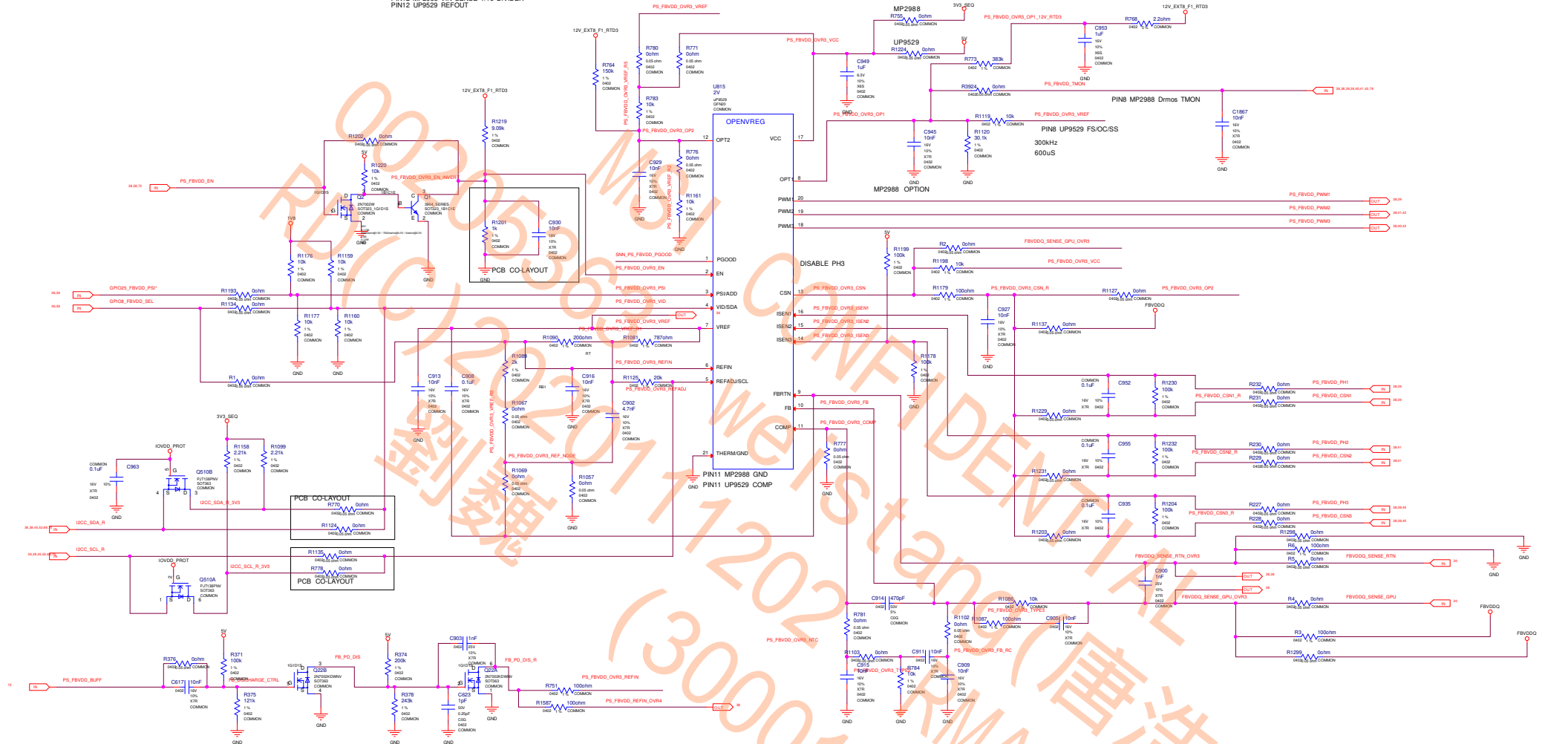


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PCB REV	PG132-A02	DATE	10-JUN-2020
BCM REV	A		

A	B	C	D	E	F	G	H
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# PS: FBVDD Controller OVR3

PIN12 MP2988 VIN SENSE 1/16 DIVIDER  
PIN12 UP9529 REFOUT



FOR DT SKU

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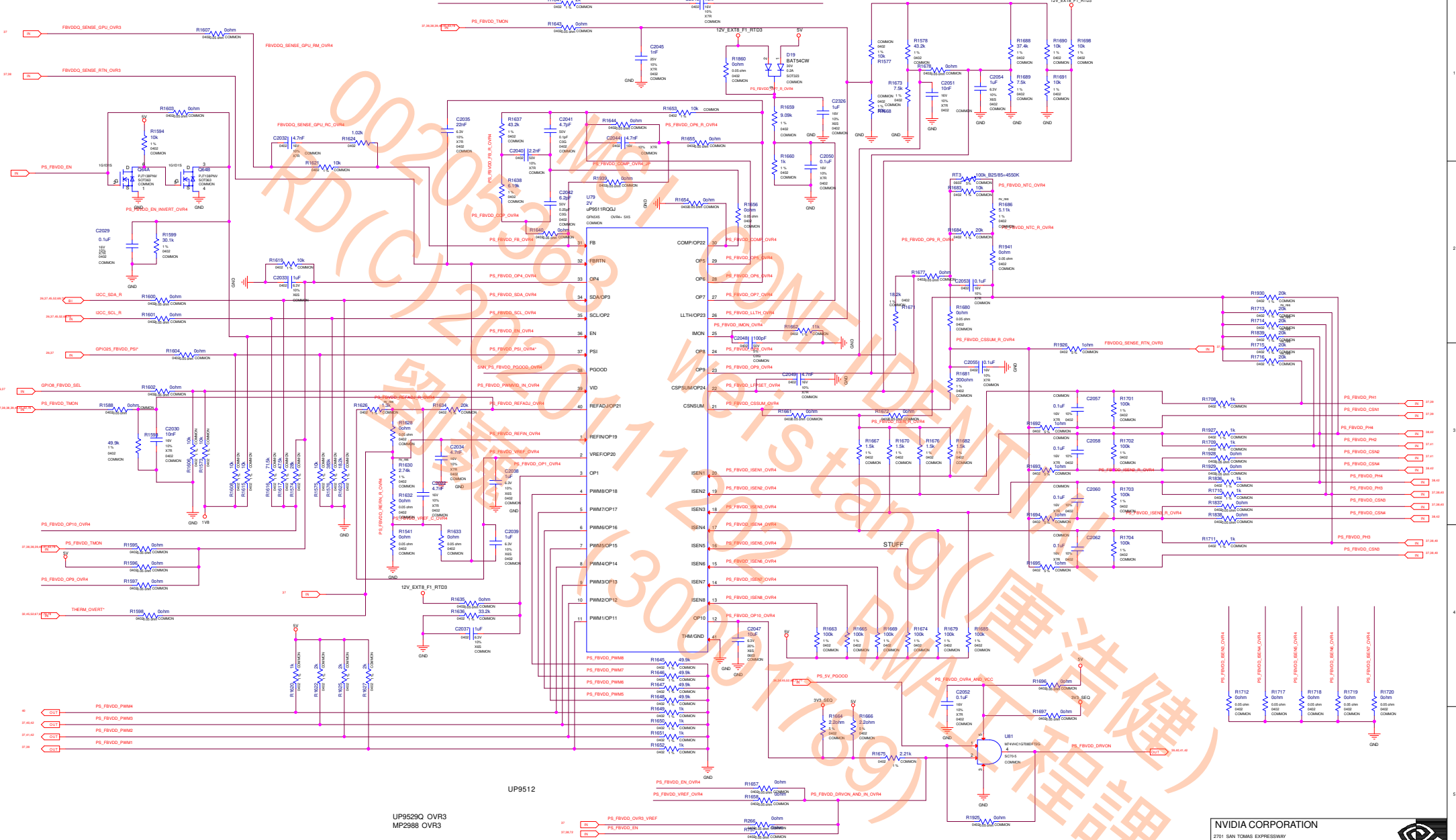
NV\_PN 600-1G132-BASE-300

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ASSEMBLY	<ASSEMBLY DESCRIPTION>
PAGE: DETAIL	PS: FBVDD CONTROLLER OVR3

## PS:FBVDDQ OVR4



UP9529Q OVR3  
MP2988 OVR3

UP9512

ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	PS: FBVDDQ CWR4

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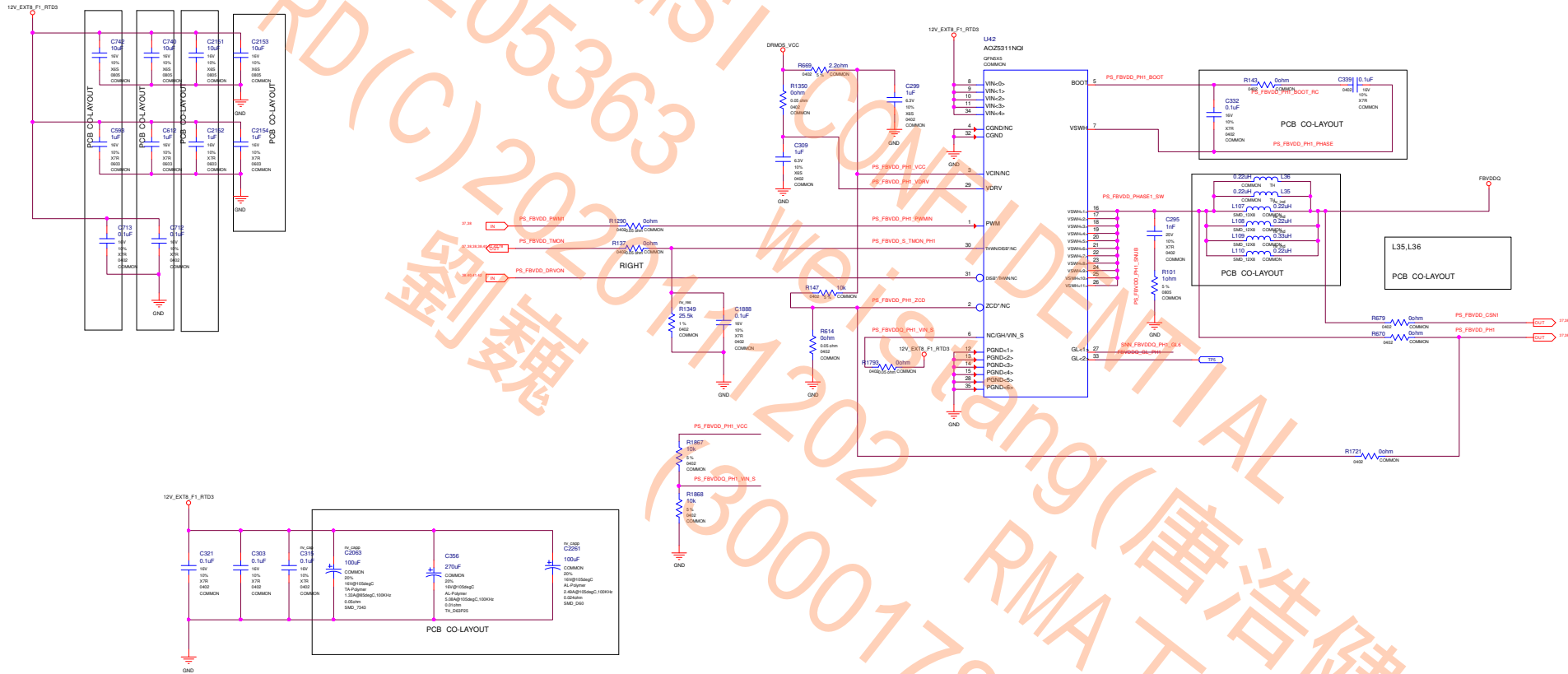


NV_PN	600-1G132-BASE-300
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PCB REV	PG132-A02	PAGE	38 OF 79
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PS: FBVDD PH1

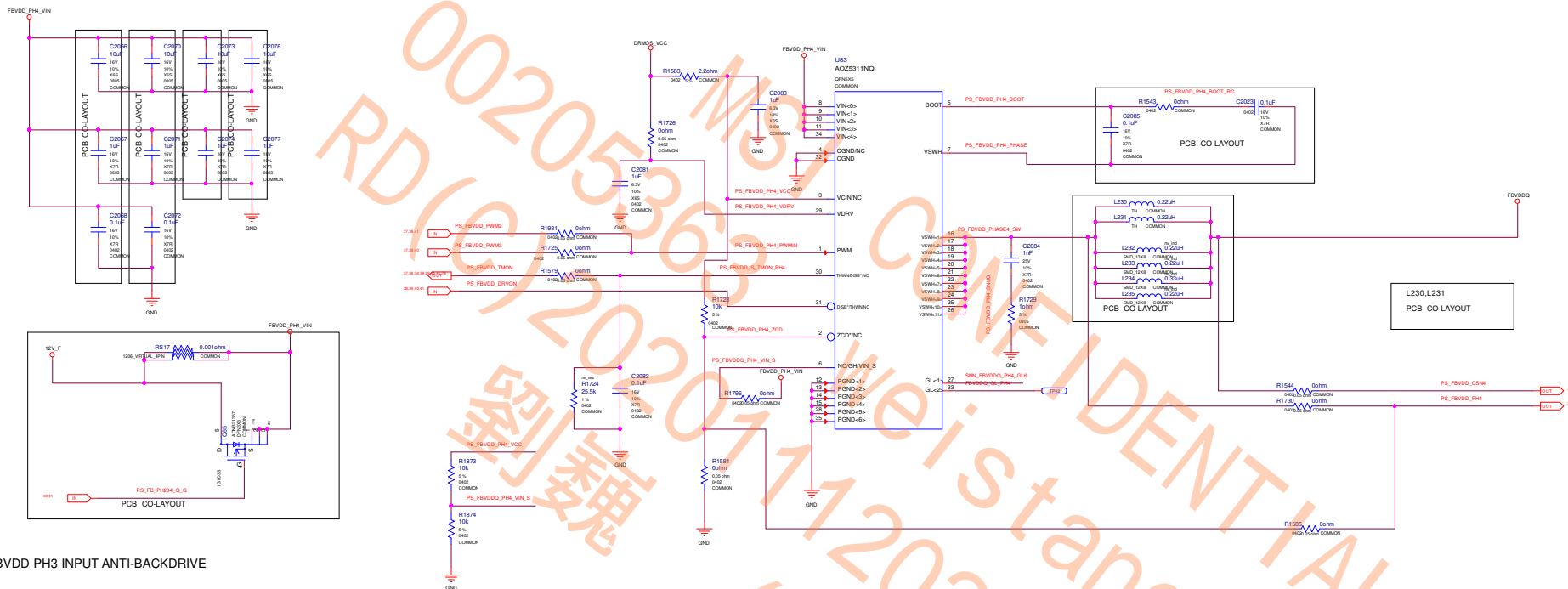




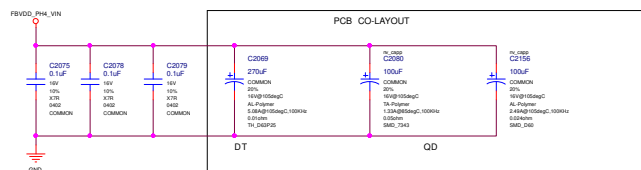




# PS: FBVDD PH4



## FBVDD PH3 INPUT ANTI-BACKDRIVE



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ASSEMBLY	ASSEMBLY DESCRIPTION
PCB CO-LAYOUT	PS: FBVDD PH4

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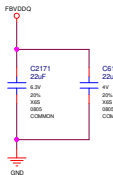
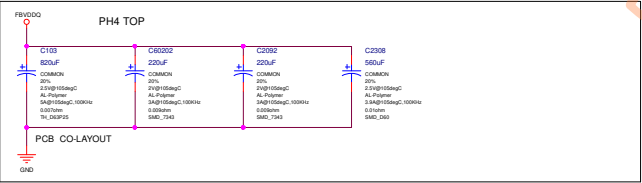
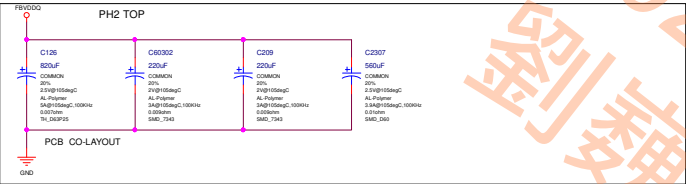


NV\_PN 600-1G132-BASE-300

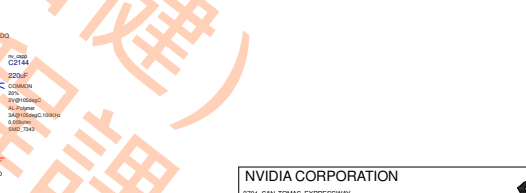
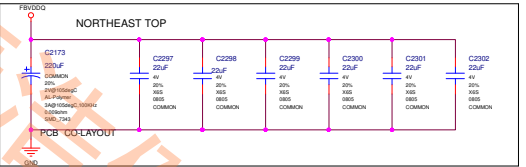
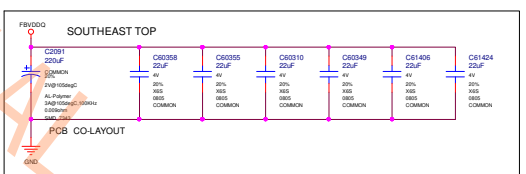
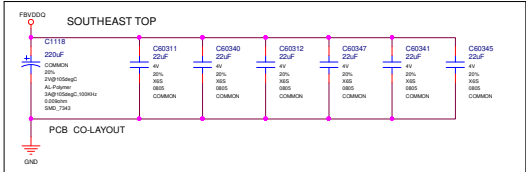
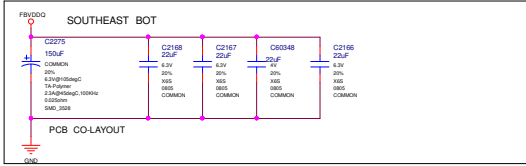
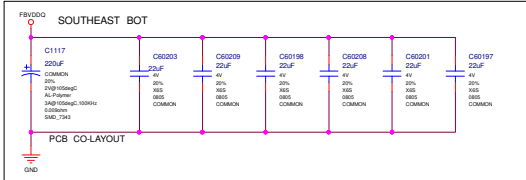
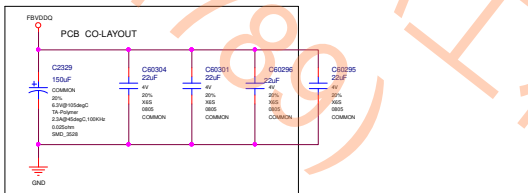
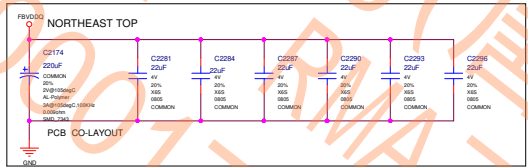
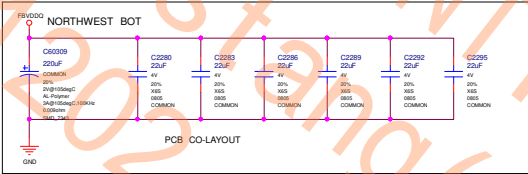
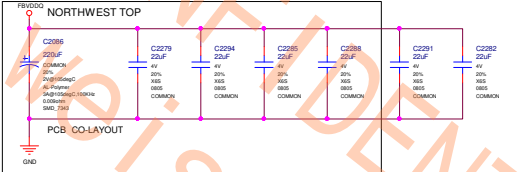
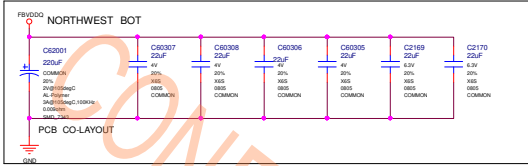
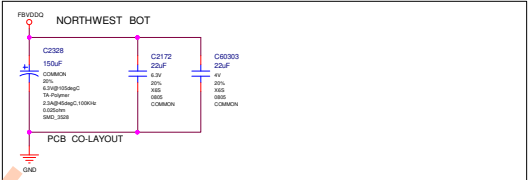
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PS: FBVDD OUTPUT CAP

3x 820uF TH FBVDD OUTPUT BULK CAPS

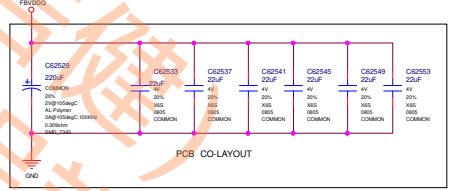
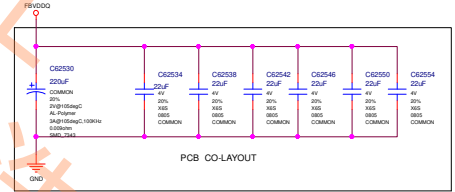
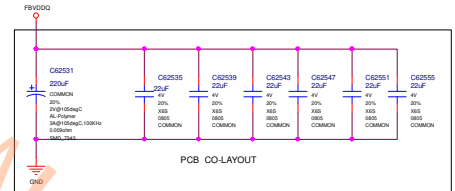
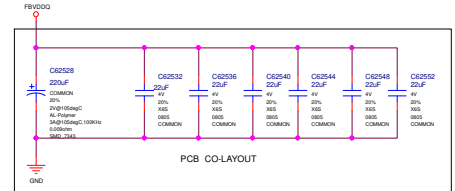
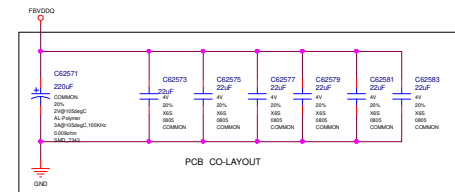
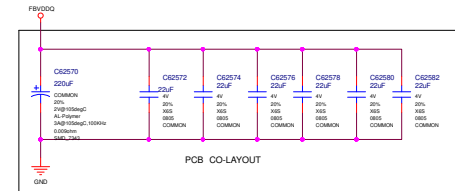
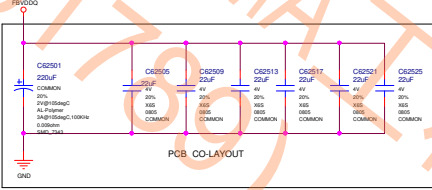
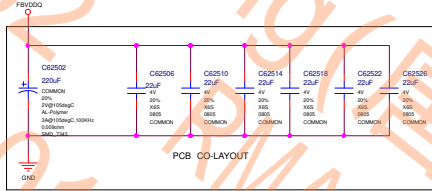
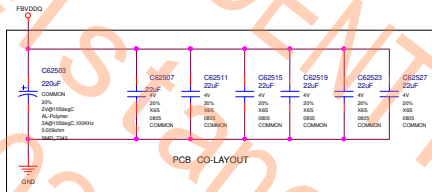
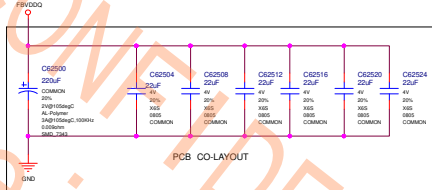
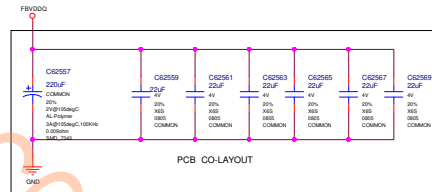
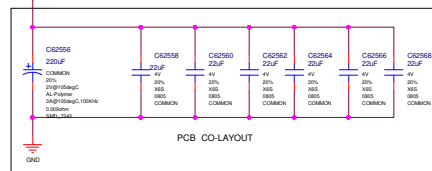


CLOSE TO FB PH3 OUTPUT STUFF



# Added for A01 x16

ADDED FOR A00 X16 DESIGN: PLACE UNDER MEMORIES



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PCB CO-LAYOUT	PCB CO-LAYOUT

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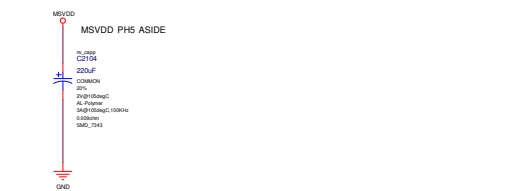
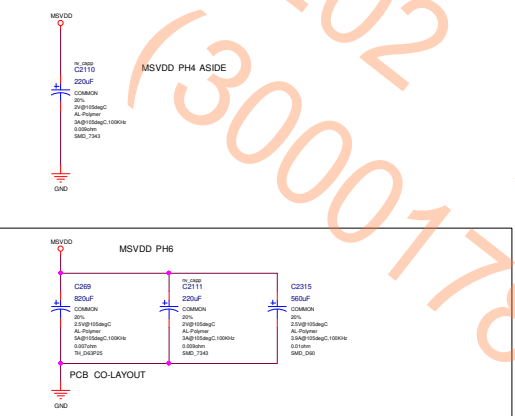
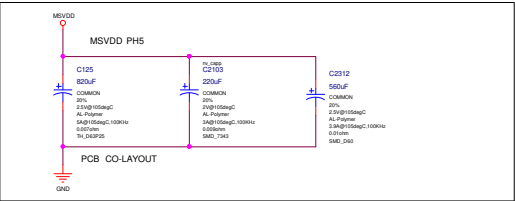
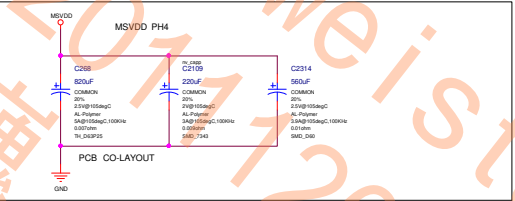
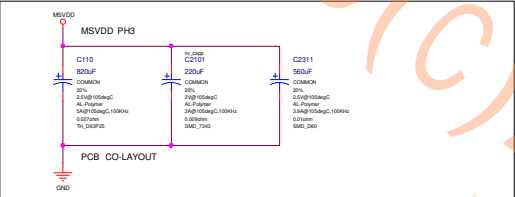
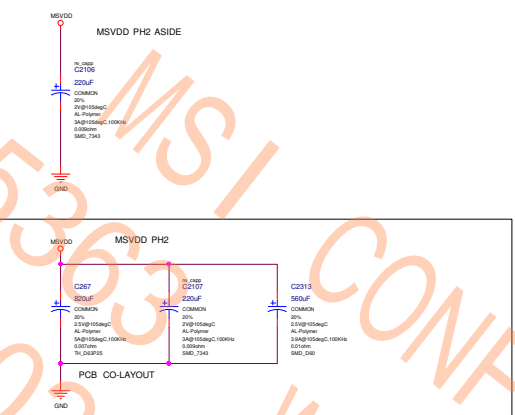
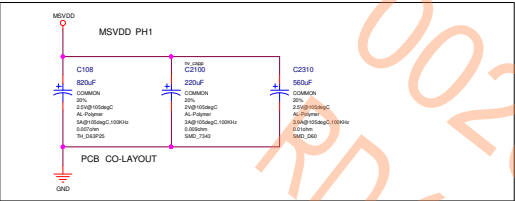








PS:MSVDD OUTPUT CAP (TOP)



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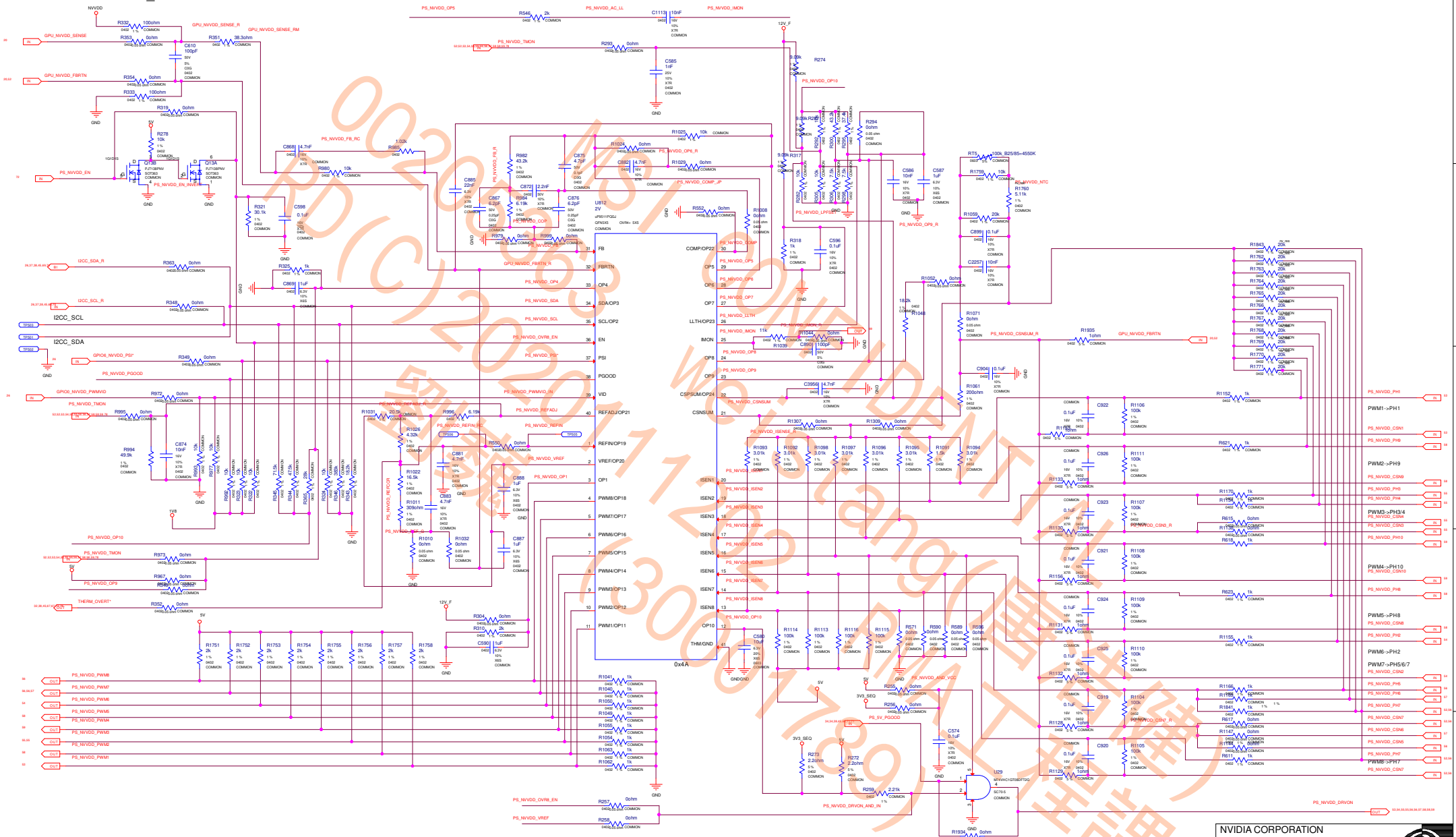
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BCM REV	A		

## PS: NVVDD Controller\_OVR8



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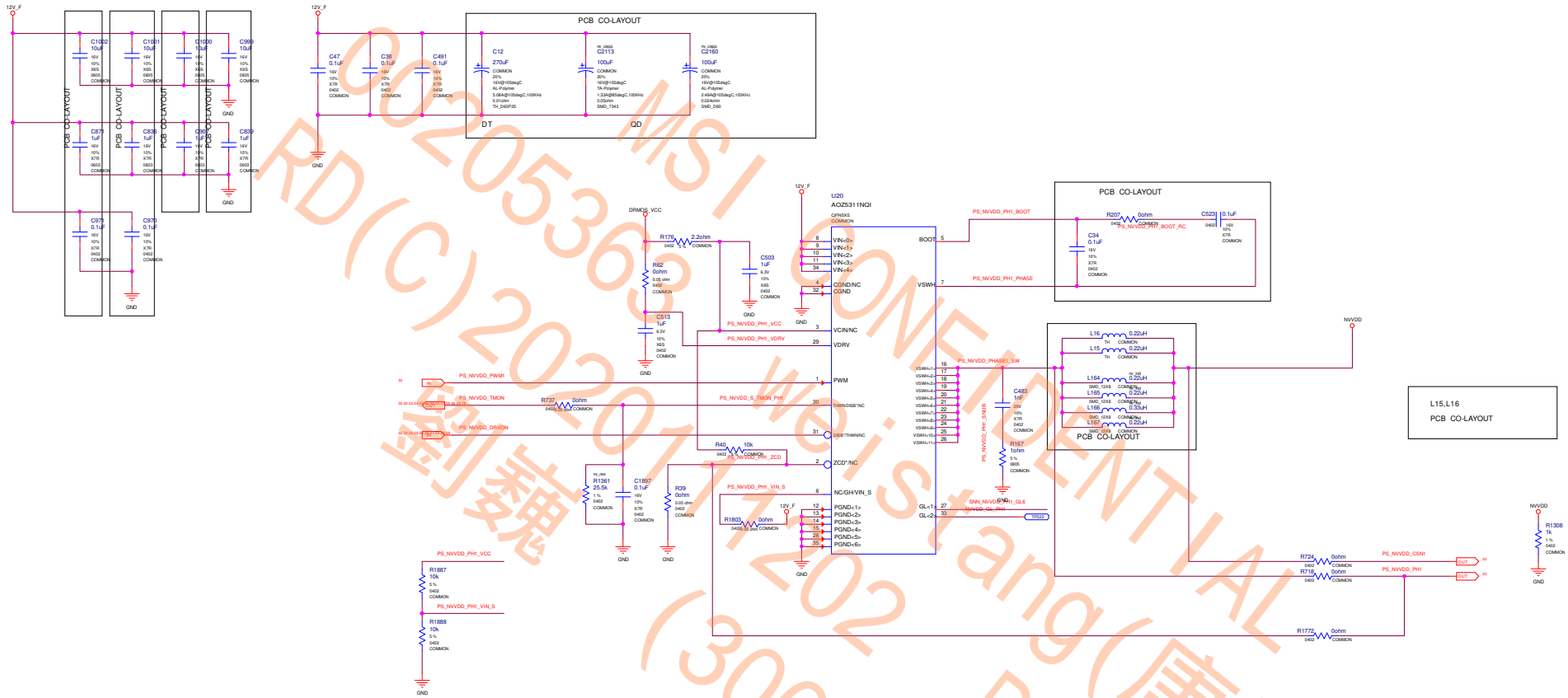
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PS: NVVDD Phase 1



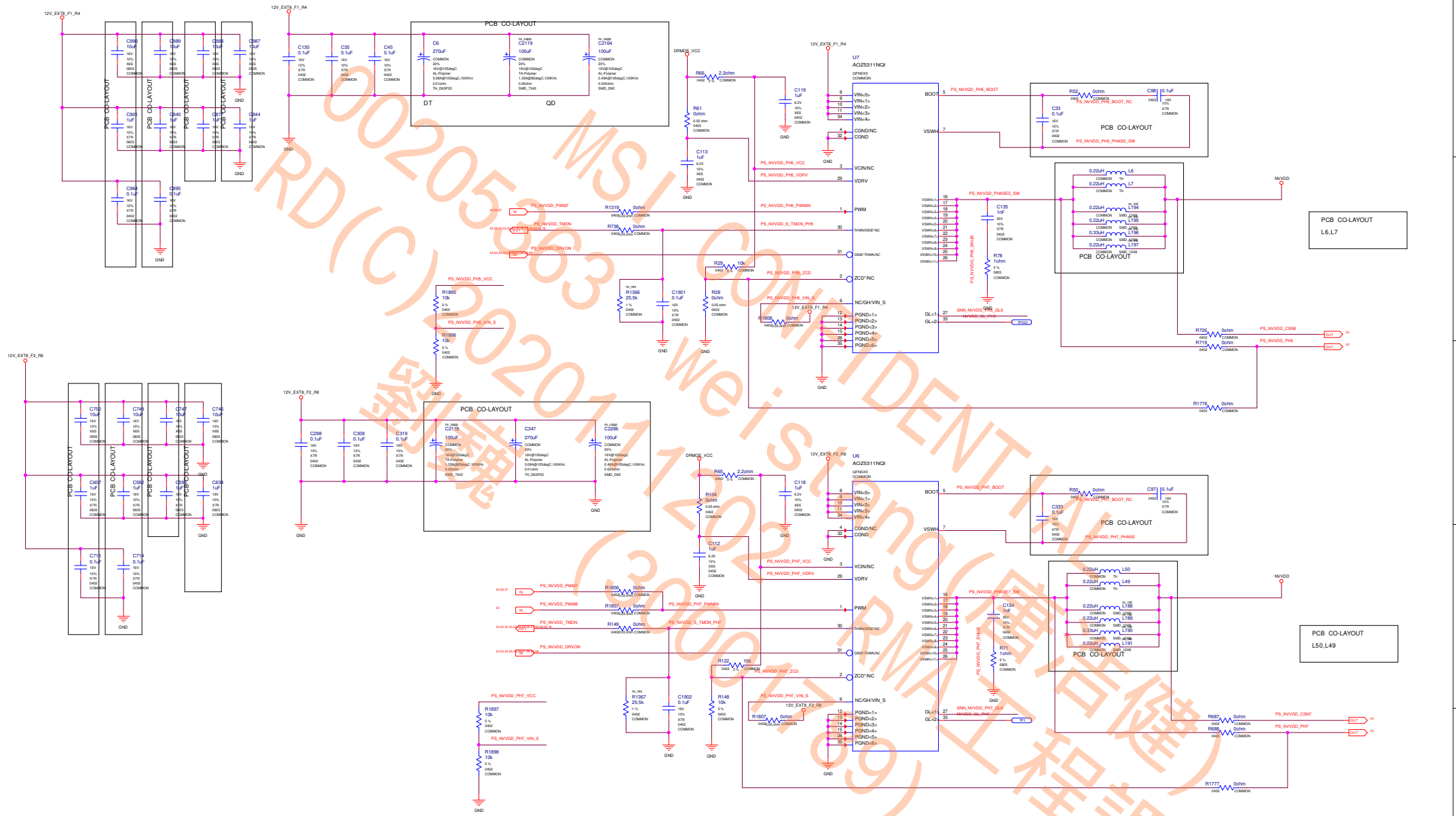
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PS: NVVDD PH 5(PWM2), PH7(PWM3)



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PCB CO-LAYOUT  
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PCB CO-LAYOUT  
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PCB CO-LAYOUT

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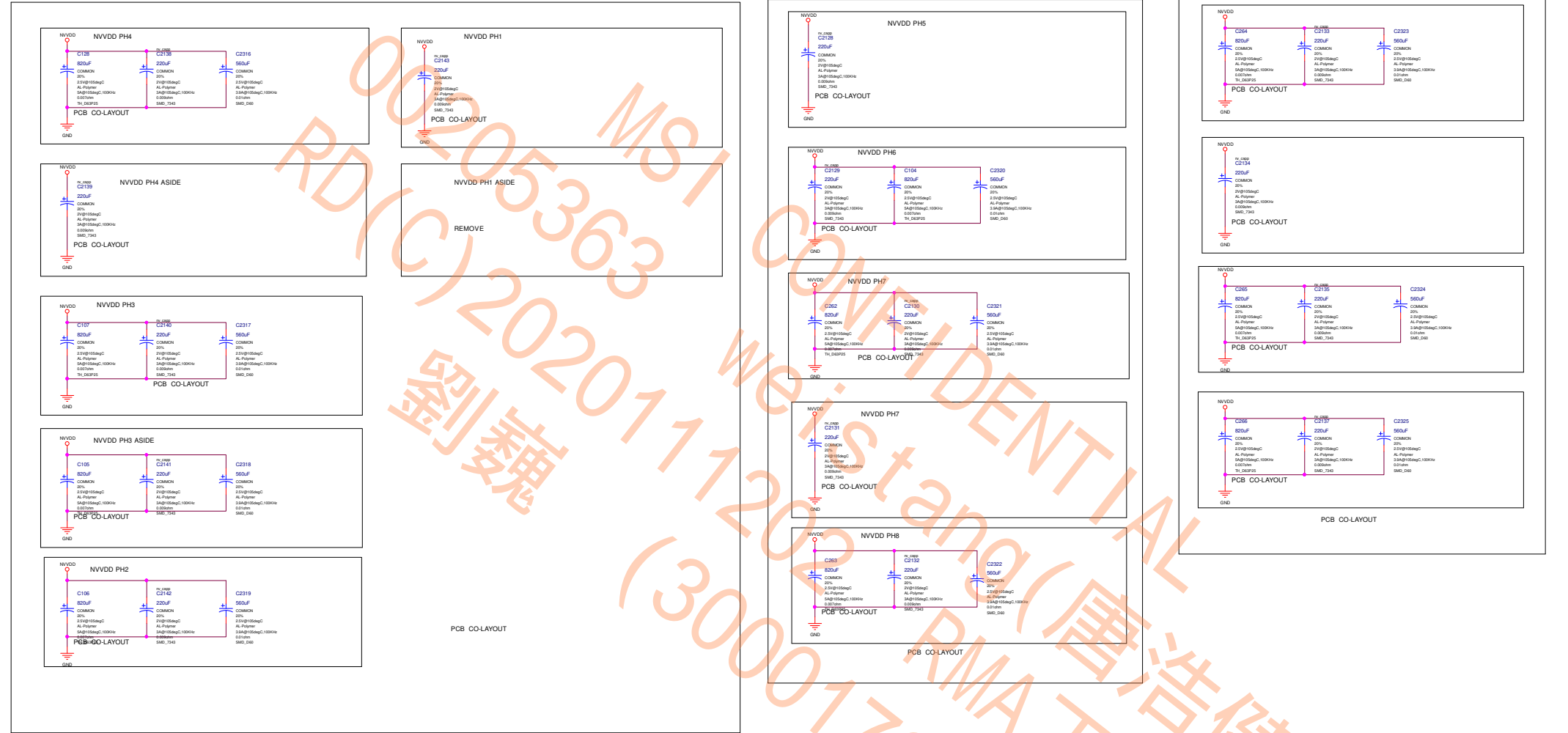
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PS: NVVDD OUTPUT CAP(TOP)




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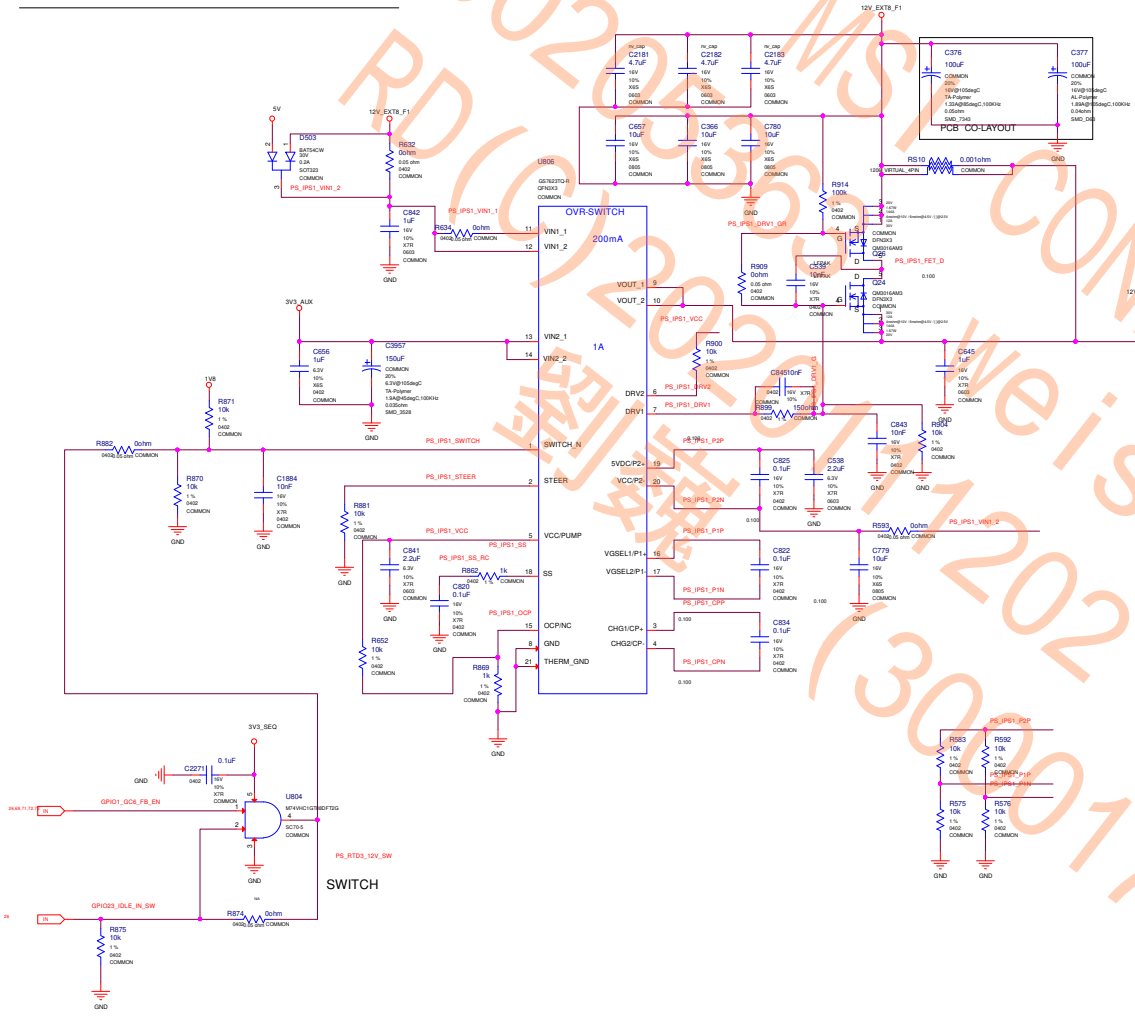
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PS: INPUT SWITCH RTD3

AND GATE LOGIC FOR P-BOARD

GPI01	GPI023	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A



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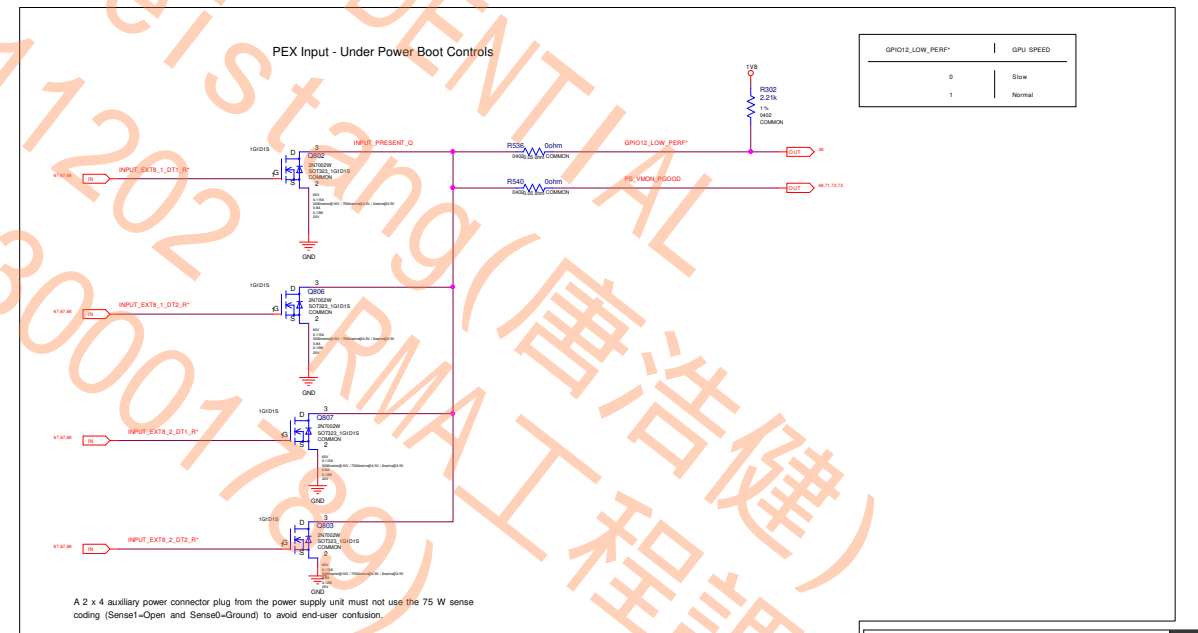
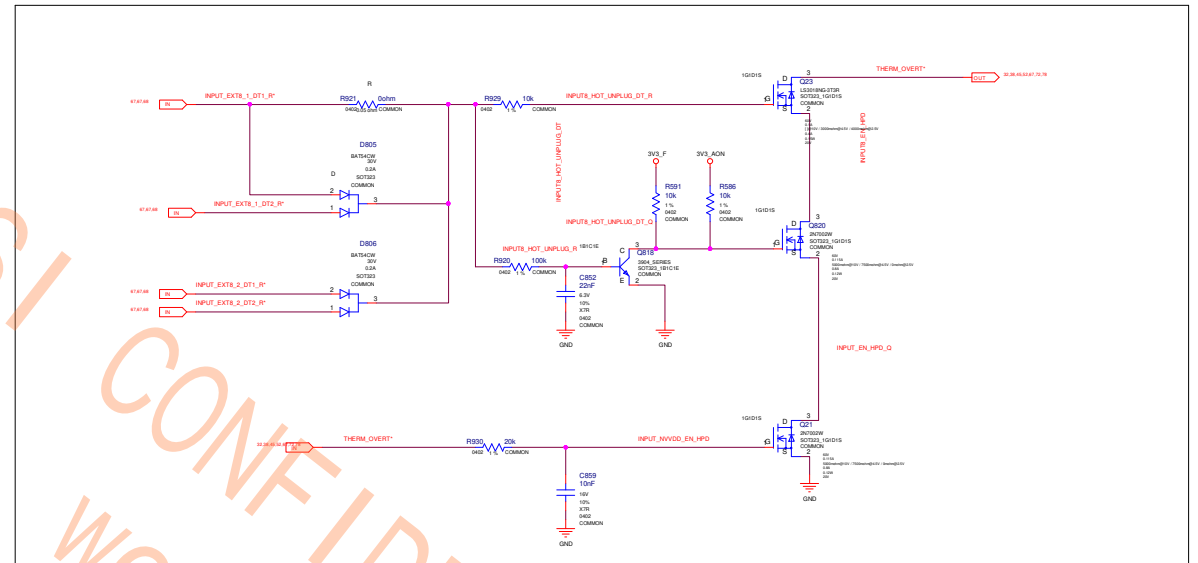
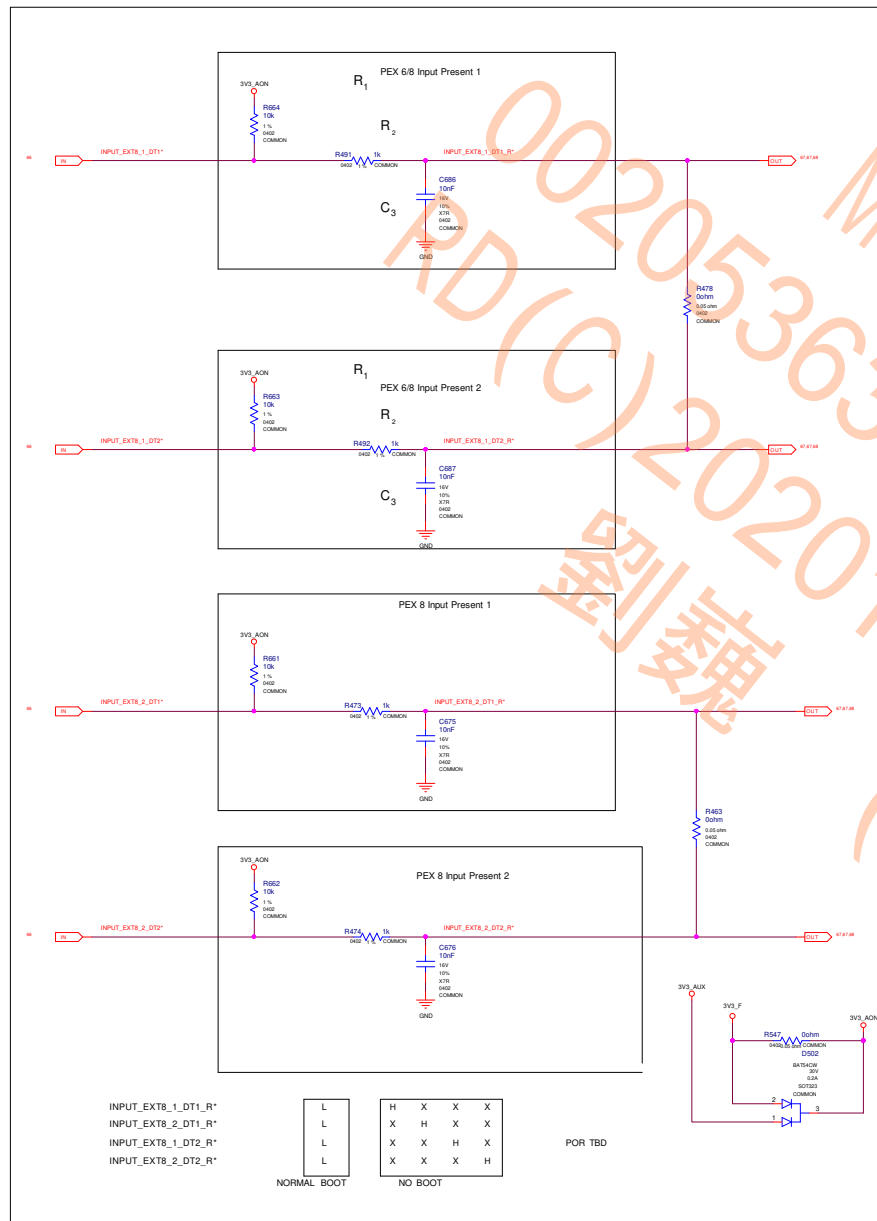
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## PS: 12V Current Steering &amp; Hot Unplug Detect



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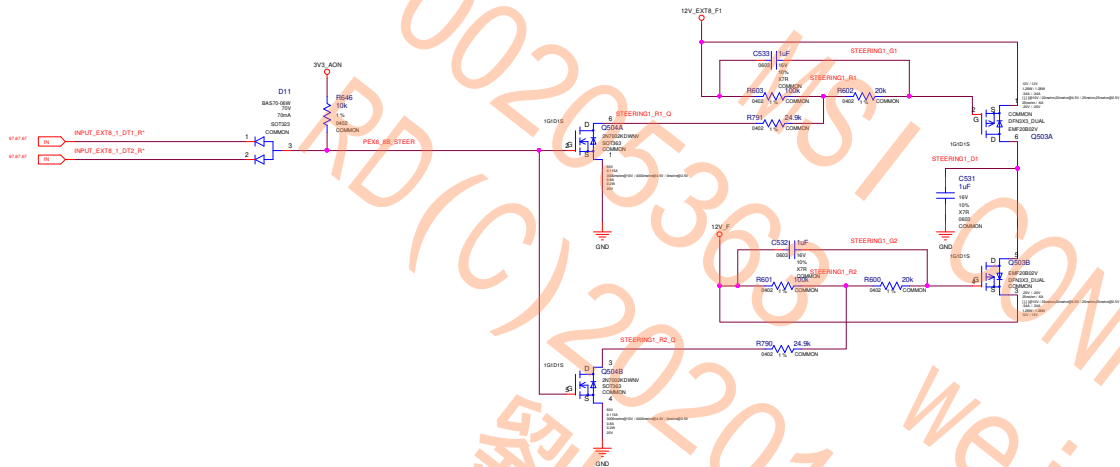
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PAGE DETAIL	PS: HOT UNPLUG



PS: Discrete Steering

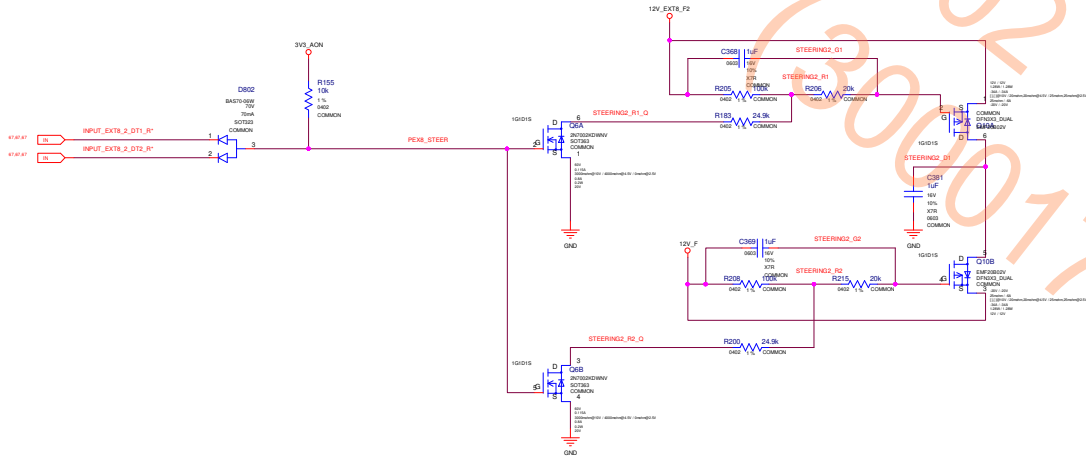
12V CURRENT STEERING (UNDER POWER BOOT):

PEX12V AND 12V\_EXT8\_F1



NO STUFF BY DEFAULT REF ONLY

PEX12V AND 12V\_EXT8\_F2



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ASSEMBLY	ASSEMBLY DESCRIPTION
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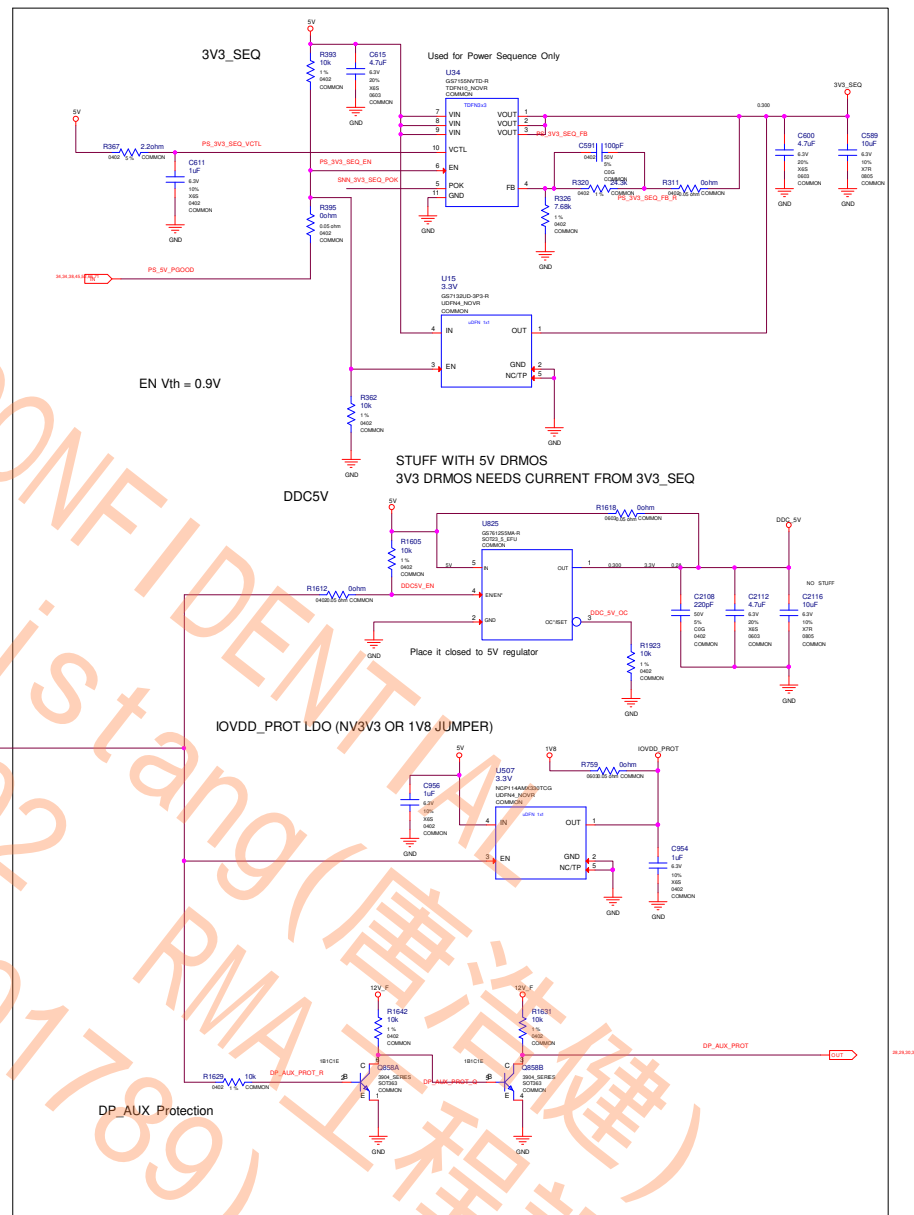
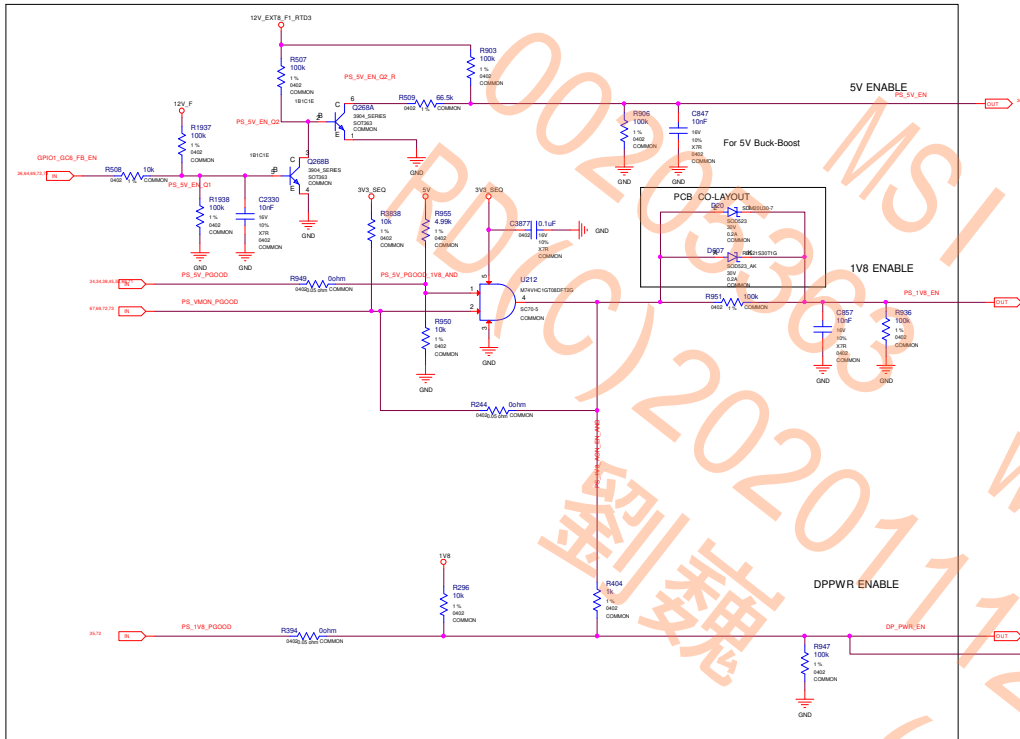




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SEQUENCE:5V,1V8,3V3\_SEQ ENABLE



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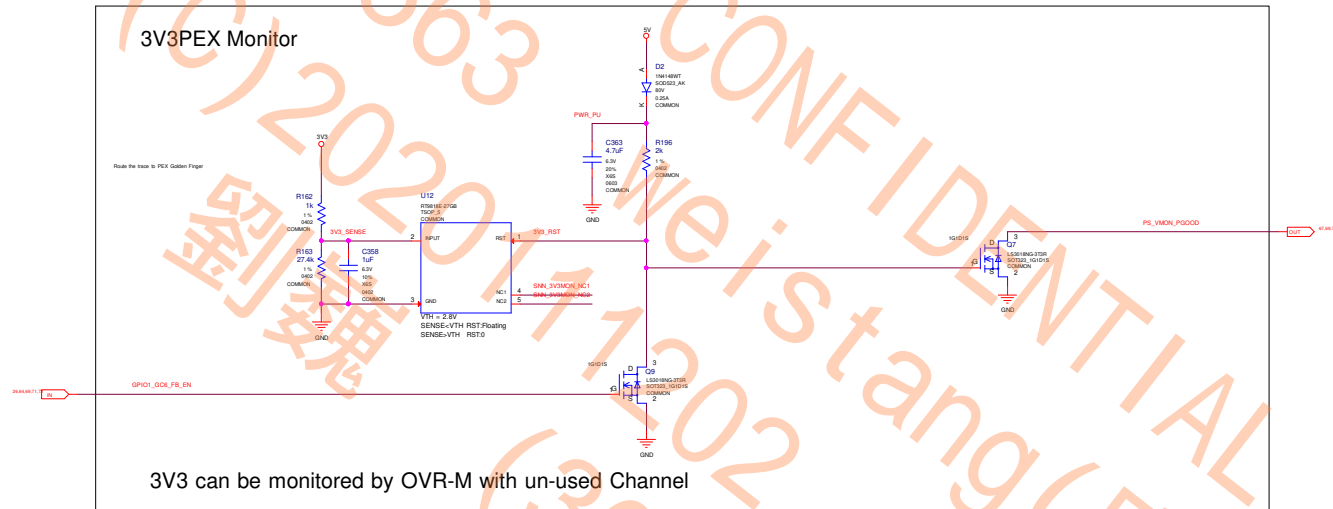
NV_PN	600-1G132-BASE-300
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3V3 can be monitored by OVR-M with un-used Channel



ASSEMBLY		«ASSEMBLY DESCRIPTION»		SANTA CLARA, CA 95050, USA	
PAGE: DETAIL		Sequence: 3/VA MONITOR			
MAY				<b>NV_PN</b> <b>600-1G132-BASE-300</b>	
DISCLAIM ALL		PCB REV		PG132-300Z	
Y STANDARDS.		ROM REV		A	
		DATE		10-JUN-2020	
				73 OF 79	

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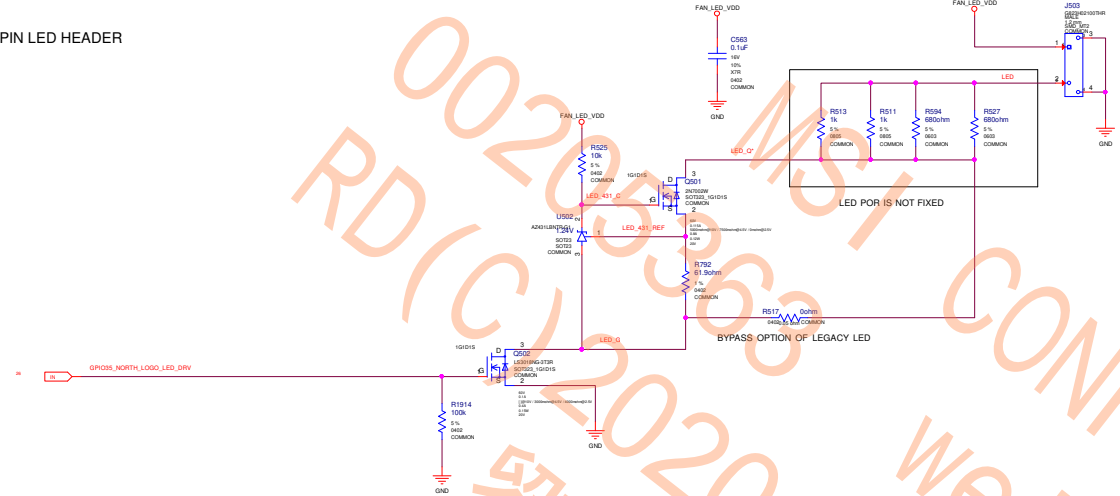
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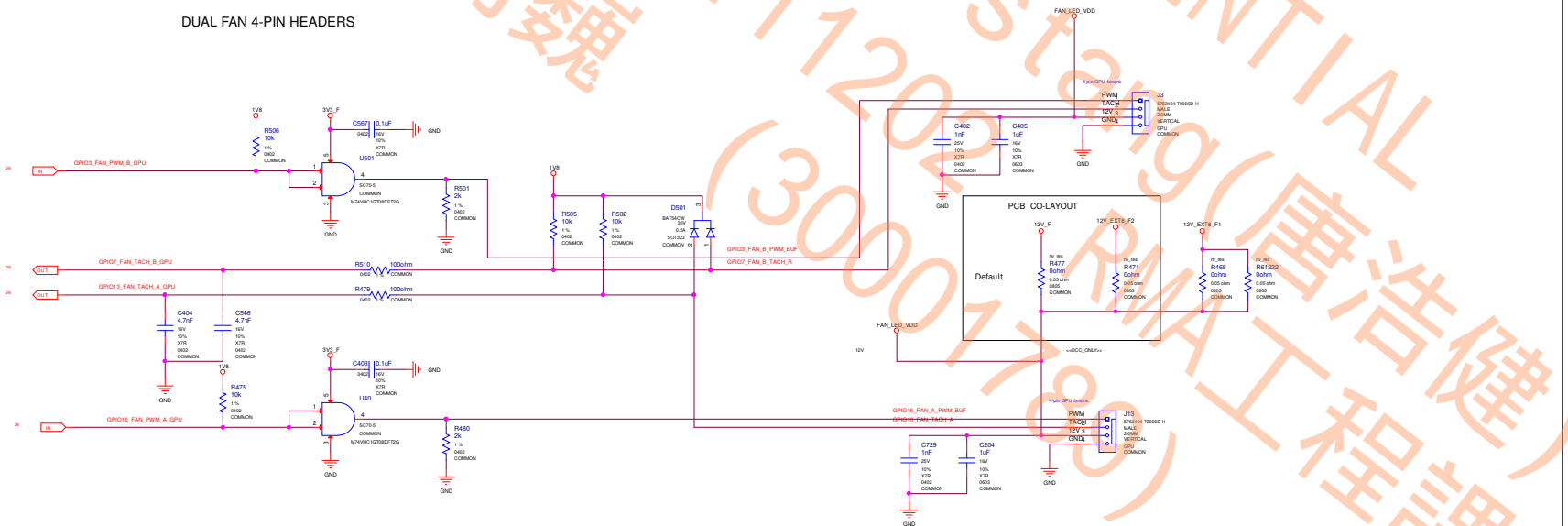




## 2-PIN LED HEADER



DUAL FAN 4-PIN HEADERS



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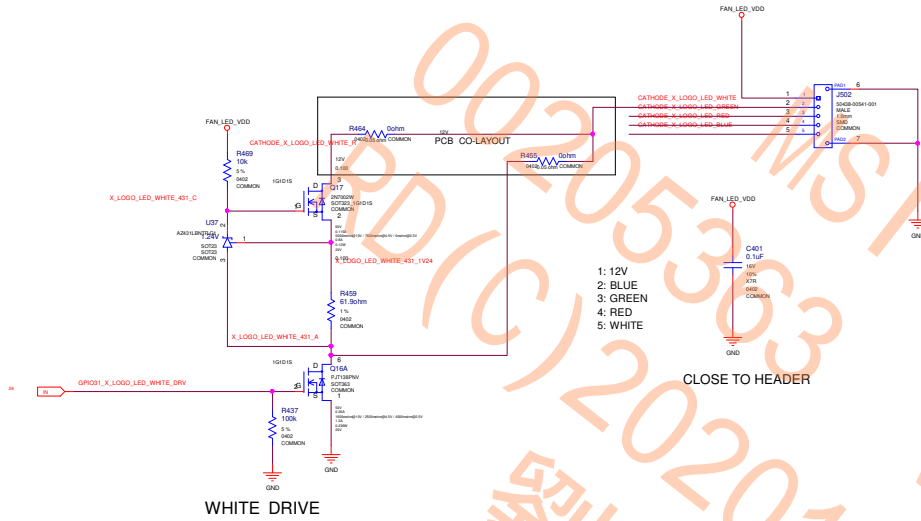
NV_PN	600-1G132-BASE-300
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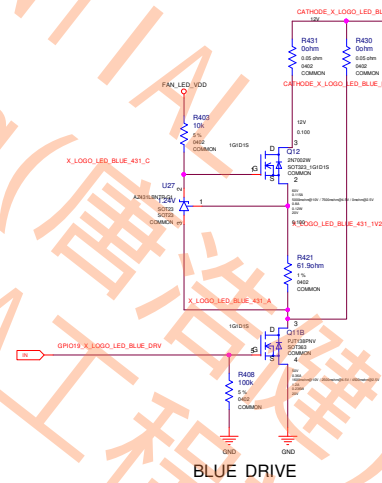
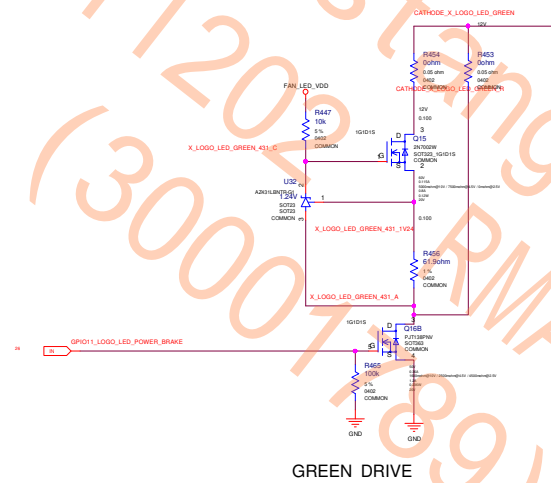
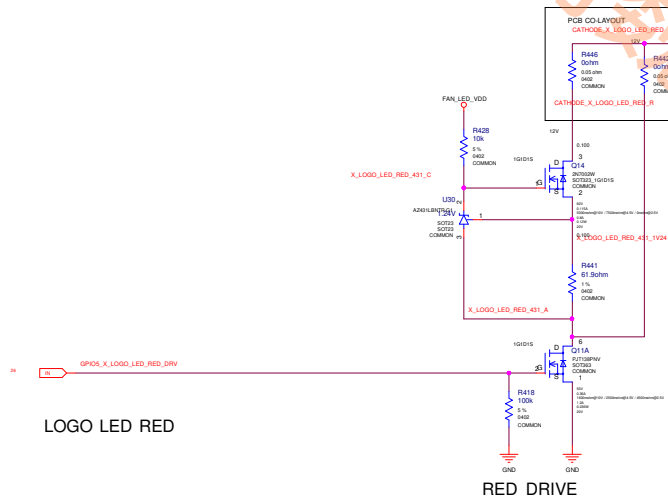
A horizontal number line with tick marks every 10 units from 0 to 100. A vertical line is drawn at the 50 mark, and the number 50 is written below the line.

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## MISC: RGBW LED REF



CONNECTOR SIZE TO FIT LAYOUT  
ALL CIRCUIT NO STUFF BY DEFAULT  
ALINGN WITH PASH  
IF ADDITIONAL POWER CONSUPTION R  
NEEDED, IT SHOULD BE ON LED MOD.



ASSEMBLY	«ASSEMBLY_DESCRIPTION»
PAGE DETAIL	RGBW LED REF

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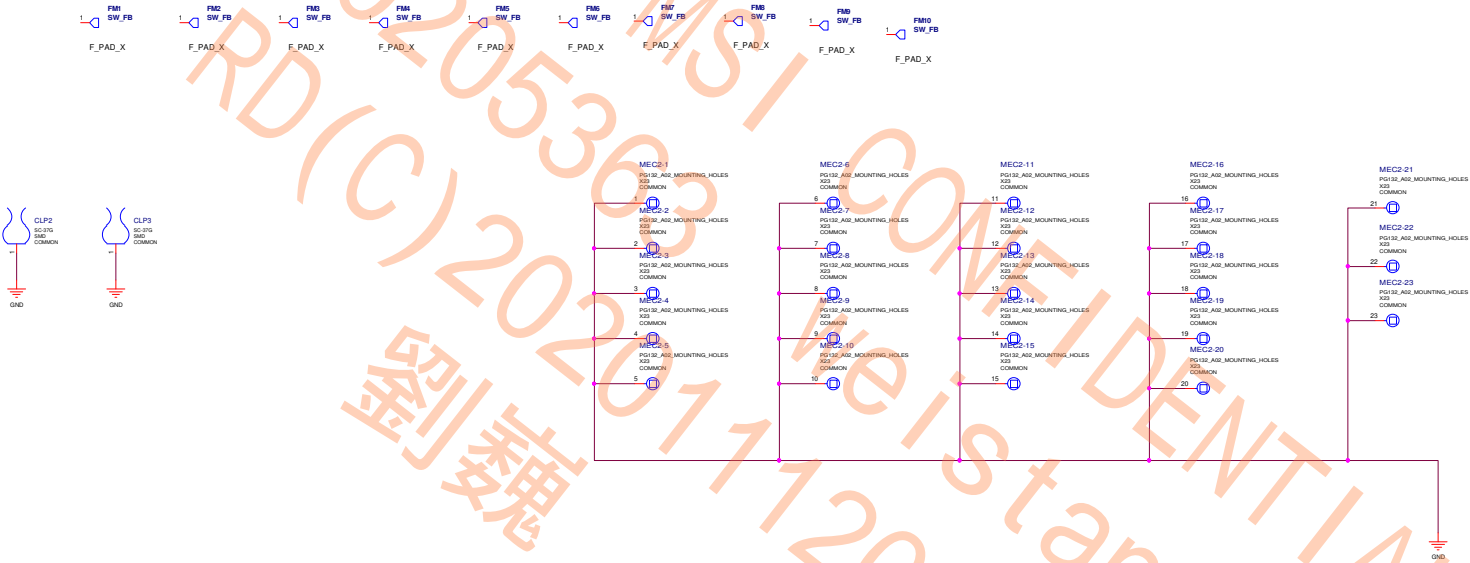


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Mechanical: Mounting holes



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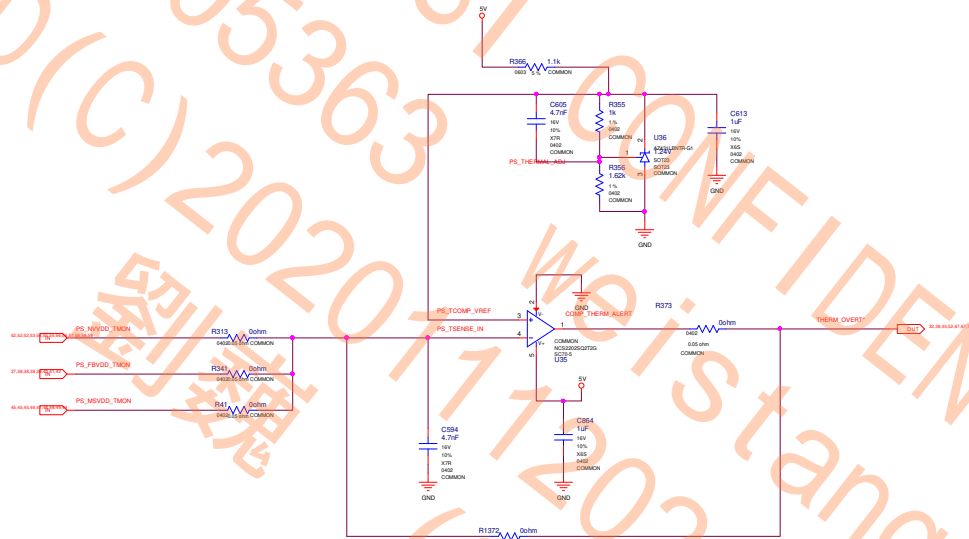
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PAGE DETAIL		MECH	
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VR THERMAL PROTECTION



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PCI TERM



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